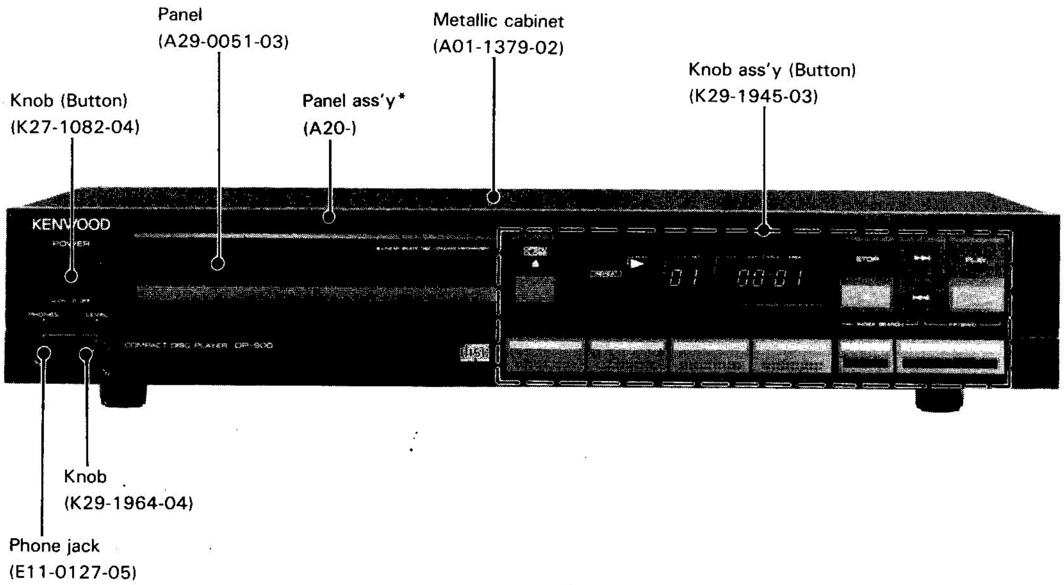
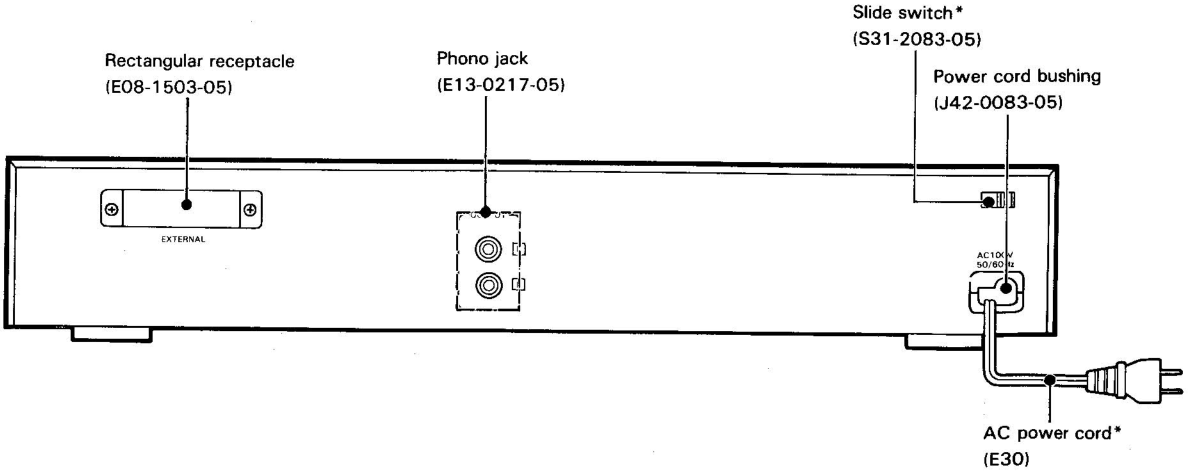
SERVICE MANUAL

KENWOOD

DP-900

COMPACT DISC PLAYER


Panel
(A29-0051-03)
Metallic cabinet
(A01-1379-02)
Knob ass'y (Button)
(K29-1945-03)
Knob (Button)
(K27-1082-04)
Panel ass'y*
(A20-)
KENWOOD
POWER
COMPACT DISC PLAYER DP-900
Knob
(K29-1964-04)
Phone jack
(E11-0127-05)


Slide switch*
(S31-2083-05)
Power cord bushing
(J42-0083-05)
Rectangular receptacle
(E08-1503-05)
Phono jack
(E13-0217-05)
EXTERNAL
AC100V
50/60Hz
AC power cord*
(E30)

TRIO-KENWOOD Corp. certifies this equipment conforms to DHHS Regulations No. 21 CFR 1040.10, Chapter I, Subchapter J.

DANGER: Laser radiation when open and interlock defeated.
AVOID DIRECT EXPOSURE TO BEAM.

Refer to Parts List on page 81.

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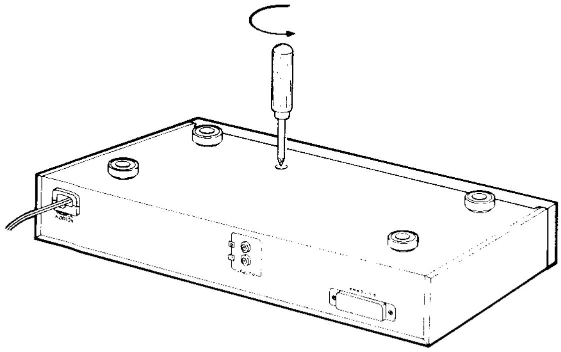
1. FUNDAMENTALS OF OPERATION

1-1. BEFORE OPERATION

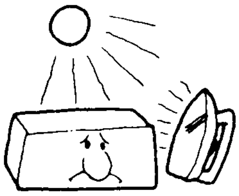
Shipping screw

Before operation, loosen the shipping screw counterclockwise by about 20 turns. The screw should be re-tightened when the unit is transported again.

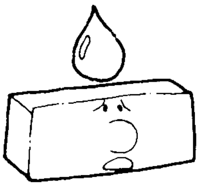


Notes on installation

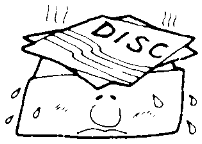
Do not place the unit in a place which is exposed to direct sunlight, near a heating appliance, etc.



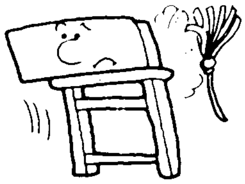
Do not place a vase containing water, makeup, etc. on the unit. Do not use in a humid place.



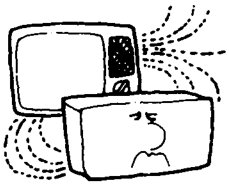
To maintain good ventilation, place the unit at least 10 cm away from the walls.



Choose a location that is relatively free from vibration or excessive dust.

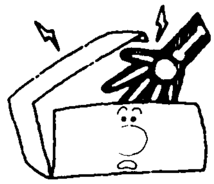


Keep the unit away from a source of magnetic fields such as TV sets, motorized toys, etc.



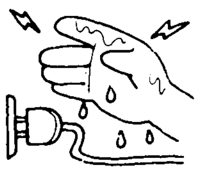
Safety precautions

Never remove the case. If the internal parts are touched accidentally, a serious electric shock might occur.



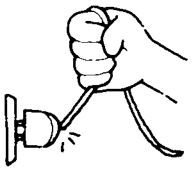
Never touch internal parts.

Touching the power plug when your hands are wet may result in a serious electric shock.



Never touch with wet hands.

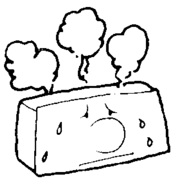
Never pull, bend or extend the power cord. This could damage the power cord, resulting in a broken cord or short-circuit.



Always grasp the plug.

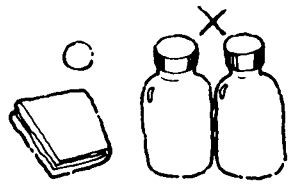
In case of abnormal smell

If an abnormal smell or smoke is detected, immediately turn the power OFF and pull out the power cord. Contact your dealer or nearest Service Station.



Cleaning

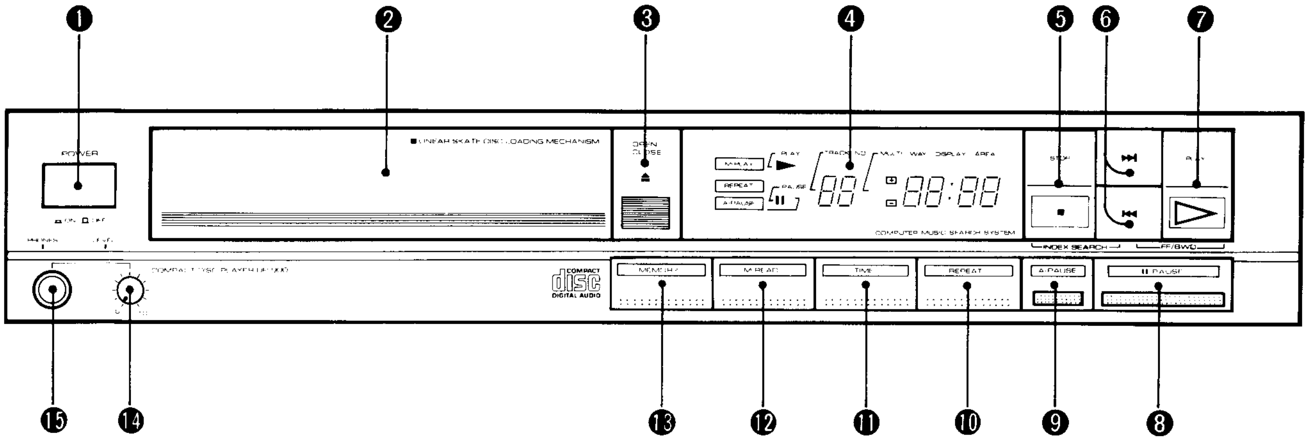
Do not use volatile solvents such as alcohol, paint thinner, gasoline, benzine, etc. to clean the cabinet. Use a silicone cloth or a clean dry cloth.



1. FUNDAMENTALS OF OPERATION

1-2. CONTROLS AND INDICATORS

Numbers in circles correspond to the diagram, abbreviations in brackets correspond to front panel indications.


❶
❷
❸
❹
❺
❻
❼
POWER
LINEAR SKATE DISC LOADING MECHANISM
OPEN CLOSE
STOP
PLAY
COMPUTER MUSIC SEARCH SYSTEM
INDEX SEARCH
FF/BWD
COMPACT disc DIGITAL AUDIO
MEMORY
REPEAT
TIME
A.PAUSE
II PAUSE
⓯
⓮
⓭
⓬
⓫
❿
❾
❽

❶ Power switch (POWER)
Press this switch to switch on the power. Press again to switch off the power.

❷ Disc tray
Load a compact disc into this tray.

❸ Open/close switch (▲ OPEN/CLOSE)
Press to open the disc tray. When this switch is pressed during play, the disc tray opens after the disc stops. Press the switch again or press the disc tray to close it. To clear the memory, also press this switch.

❹ Mode display

- **Memory play indicator (M-PLAY)**
Lights during memory play.
- **Track No. indicator (TRACK NO.)**
Displays the track No.
- **MULTI WAY DISPLAY AREA**
Displays the playing time of the selection being played, total playing time of the disc (+) or remaining playing time (−) in minutes and seconds. The index No. is displayed in index search of memory channel Nos.
- **Repeat indicator (REPEAT)**
Lights when the repeat switch (REPEAT) is pressed, indicating that the unit is in repeat mode.
- **Play indicator (▶ PLAY)**
Lights when the play switch (▷ PLAY) is pressed.
- **Pause indicator (❚❚ PAUSE)**
Lights when the pause switch (❚❚ PAUSE) is pressed.
- **Auto-pause indicator (A-PAUSE)**
Lights when the auto pause switch (A-PAUSE) is pressed.

❺ Stop switch (■ STOP)
Press this switch to release the operation mode. The laser pickup returns to the start position, the unit enters the standby mode.

❻ Music search switches (⏮, ⏭)

- **During play and pause**
When the music search switch (⏭) is pressed, the next selection is selected. When the music search switch (⏮) is pressed, the beginning of the current selection is selected. When the switch is pressed again, the track No. indicator (TRACK NO.) shows the beginning of the previous selection. When the switch is kept pressed, proceeding or previous selection can be selected.
- **During memory play**
When the music search switch (⏭) is pressed, the beginning of the next memorized selection is displayed in the MULTI WAY DISPLAY AREA and selected. When the music search switch (⏮) is pressed, the selection previously memorized is displayed in the MULTI WAY DISPLAY AREA and selected. When the switch is kept pressed, the proceeding or previous memorized selection can be selected.
- **To skip ahead**
Keeping the play switch (▷ PLAY) pressed, press the music search switch (⏭) to skip a selection.
- **To go backward**
Keeping the play switch (▷ PLAY) pressed, press the music search switch (⏮) to go backward.
- **Index search**
Set the unit to standby mode and select the desired track No. with the music search switch. While the desired track No. is dispalyed, press the music search switch while keeping the stop switch (■ STOP) pressed to select the index No.
For example, to select index No. 2 of the third selection, press the stop switch (■ STOP) and press the music search switches (⏮ ⏭) to select track No. 3. Keeping the stop switch (■ STOP) pressed, press the (⏮ ⏭) switch to display "03 : 02".
Press the play switch (▷ PLAY) to start play from index No. 2 of the third selection.

1. FUNDAMENTALS OF OPERATION

❼ Play switch (▷ PLAY)
When this switch is pressed, the play indicator (▷ PLAY) lights and play starts. When the track No. is selected with the music search switches (⏮ ⏭) in playback standby mode, pressing this switch will start play at the beginning of the selected selection. When this switch is pressed after the memory read switch (M-READ) is pressed to select the desired selection, the memorized selections are played in turn. (memory play).

❽ Pause switch (❚❚ PAUSE)
When this switch is pressed during play, the pause indicator (❚❚ PAUSE) lights and play temporarily stops. To resume play, press the play switch (▷ PLAY). When this is pressed after selecting the track No. with the music search switches (⏮ ⏭) in playback.standby mode, the unit enters pause mode at the beginning of the selected selection.

When this switch is pressed after the memory read switch (M-READ) is pressed, the unit enters pause mode at the beginning of the selected memorized selection.

❾ Auto pause switch (A-PAUSE)
When this switch is pressed during play, play of the current selection stops and the unit enters pause mode at the beginning of the next selection.

To release auto pause mode, press the switch again.

❿ Repeat switch (REPEAT)
Press to repeat a tune. The repeat indicator (REPEAT) lights and all tunes will be played in the manual play mode. In the memory play mode, all the tunes stored in memory will be played back. Press this switch again to release the repeat mode. The repeat indicator (REPEAT) goes off.

⓫ Time switch (TIME)
During play, the MULTI WAY DISPLAY AREA displays the playing time of the selection currently being played back. When this switch is pressed, the MULTI WAY DISPLAY AREA shows the total playing time (+) of the disc.

When this switch is pressed again, the MULTI WAY DISPLAY AREA shows the remaining time (–).

In the standby mode, the MULTI WAY DISPLAY AREA shows 00:00. When the time switch (TIME) is pressed, ⊞00:00 is displayed. When the time switch (TIME) is pressed again, the total playing time of the disc is displayed. When the memory read switch (M-READ) switch is pressed, the MULTI WAY DISPLAY AREA shows the channel No. When the time switch (TIME) is pressed, the total elapsed playing time of the memorized selection is displayed.

Note:
When the total playing time of the memorized selections is more than 99 minutes or 20 or more selections of the disc which contains more than 20 selections are memorized, the MULTI WAY DISPLAY AREA shows – – : – –.

⓬ Memory read switch (M-READ)
Each time this switch is pressed, the track No. indicator (TRACK NO.) shows the track number and MULTI WAY DISPLAY AREA shows the memory channel No. or total playing time of the memorized selection for about 3 seconds in turn.

To clear all memorized selections, press the open/close switch (▲ OPEN/CLOSE).

⓭ Memory switch (MEMORY)
Press this switch to store the displayed track No. When this switch is pressed during play, the track No. of the selection being played is memorized. Up to 16 selections can be memorized.

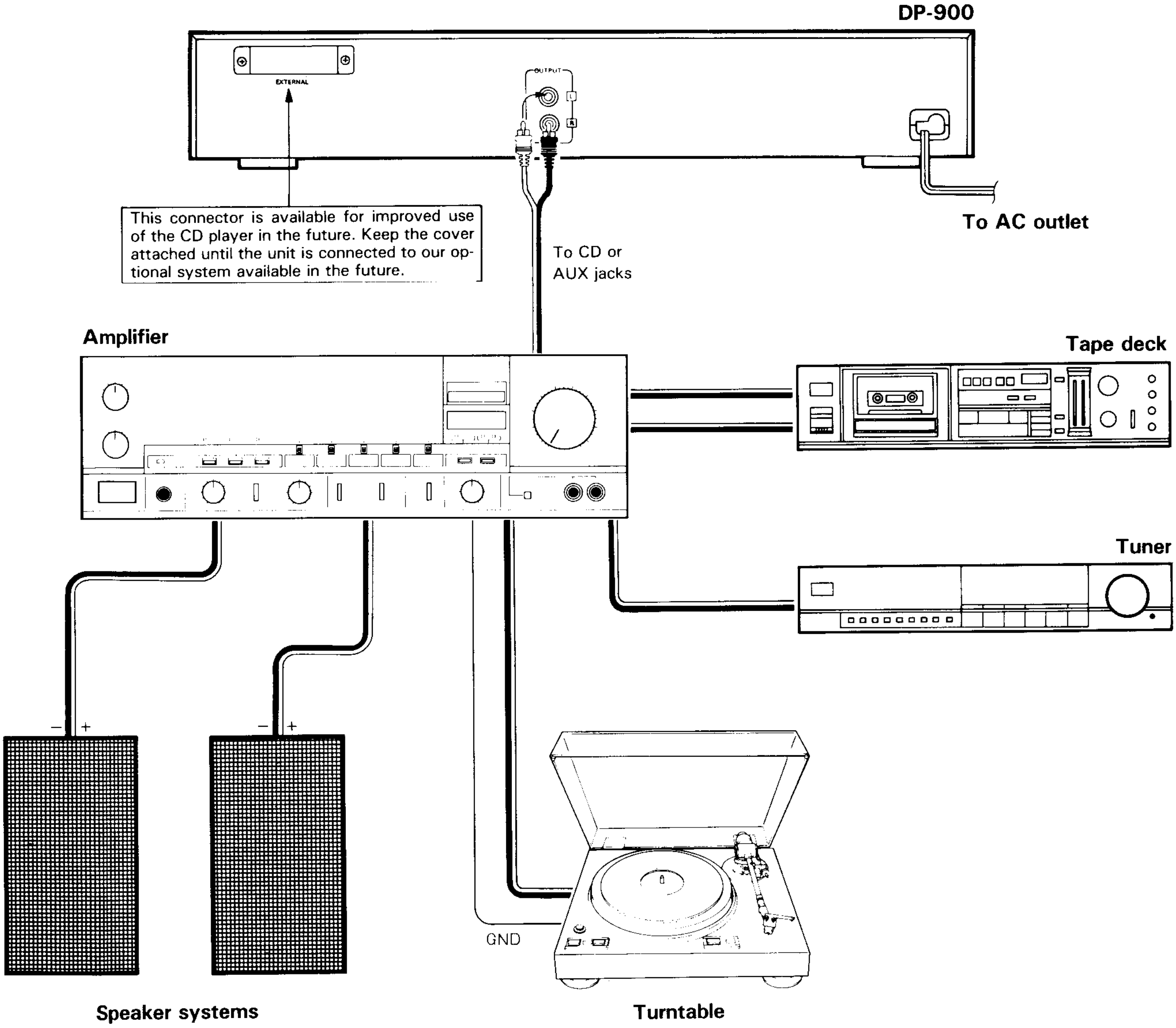
⓮ Headphones level control (PHONES LEVEL)
Used to adjust the output level of the headphones. When this control is turned clockwise, the output level increases.

⓯ Headphones jack (PHONES)
Connect the headphones plug to this jack.

1. FUNDAMENTALS OF OPERATION

1-3. SYSTEM CONNECTIONS

- Make system connections with the power turned off.


DP-900
EXTERNAL
OUTPUT
This connector is available for improved use of the CD player in the future. Keep the cover attached until the unit is connected to our optional system available in the future.
To CD or AUX jacks
To AC outlet
Amplifier
Tape deck
Tuner
GND
Speaker systems
Turntable

Power cord connection

Connect the power cord to a convenient AC outlet.

Connection to the amplifier

Connect the output jacks (OUTPUT) to the right and left CD, TUNER, TAPE IN or AUX jacks of the amplifier.

Note:

Do not connect the output jacks to the PHONO jacks of the amplifier.

1. FUNDAMENTALS OF OPERATION

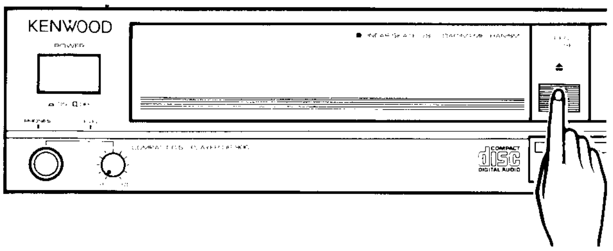
1-4. OPERATING INSTRUCTIONS

How to load a compact disc

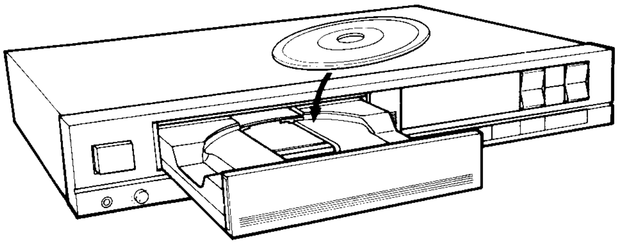
1 Set the power switch (POWER) to ON.
2. Take out the compact disc from its case.
3. Press the open/close switch (▲ OPEN/CLOSE) to open the disc tray and insert the disc with the label facing upward.

Notes:

1. Take care not to insert the disc back upside down.
2. Never insert anything other than a disc into the disc tray.



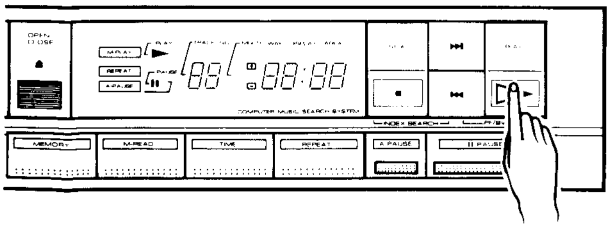
4. Press the open/close switch (▲ OPEN/CLOSE) to close the disc tray. The disc starts rotating automatically. For the first few seconds, the information recorded at the beginning of the disc is read and switch operation is not possible.
5. When the information is read, the unit enters play standby mode and the mode display shows "0 1 00:00".



Manual playback

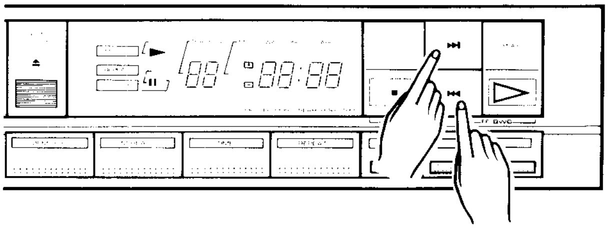
■ How to play back from the first tune

1. Set the power switch (POWER) to ON.
2. Load a compact disc in the disc tray.
3. When the mode display shows "0 1 00:00", press the play switch (▷ PLAY). The play indicator (▶ PLAY) lights and play starts at the beginning of the disc.
4. After play backing the last tune, the laser pickup returnes to the beginning of the first tune and the unit enters the standby mode.



■ How to search the next or previous tune (Music search)

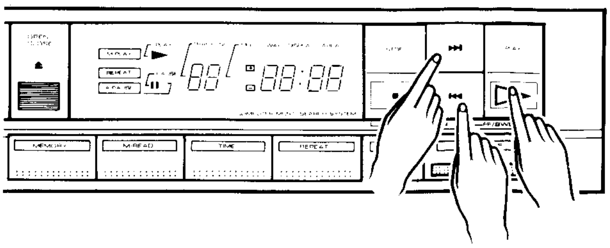
1. To play back the next tune, press the music search switch (▶▶|) once. The next tune No. displayed in track No. indicator (TRACK NO.) lights. When the unit is in the playback mode, pressing the music search switch (▶▶|) will start the playback from the beginning of the next tune. When the music search switch (▶▶|) is pressed in the pause mode, the unit enters the pause mode at the beginning of the next tune. To play back the next tune, press the play switch (▷ PLAY).
2. By pressing the music search switch (▶▶|) more than once or keeping the switch pressed, any subsequent tune can be selected. Select the tune while observing the track No. displayed in the track No. indicator (TRACK NO.).
3. To play back the previous tune, press the music search switch (|◀◀). During playback, the unit returns to the beginning of the current tune. Immediately press the switch again to return the unit to the beginning of the previous tune.
4. Press the music search switch (|◀◀) repeatedly or continuously to select the previous tune, observing the track No. indicator (TRACK NO.).



■ Tune selection play

1. Select the track No. of the desired selection with the music search switches (|◀◀ ▶▶|). The track No. indicator (TRACK NO.) shows the selected track No. To select the index No., refer to "Index search" of Music search switches (|◀◀ ▶▶|) (6) on page 5 .
2. Press the play switch (▷ PLAY). The play indicator (▷ PLAY) lights and the unit starts playing back the selected tune.

When the unit is set to play mode, the playback of the selected tune starts after step 1.

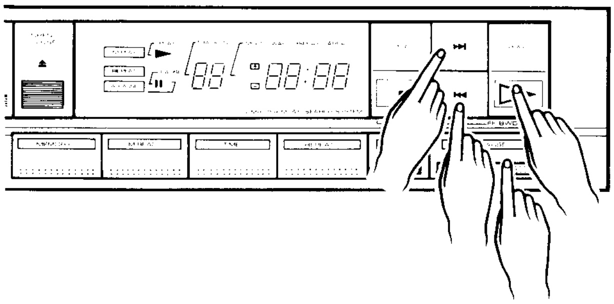


1. FUNDAMENTALS OF OPERATION

■ Tune selection pause

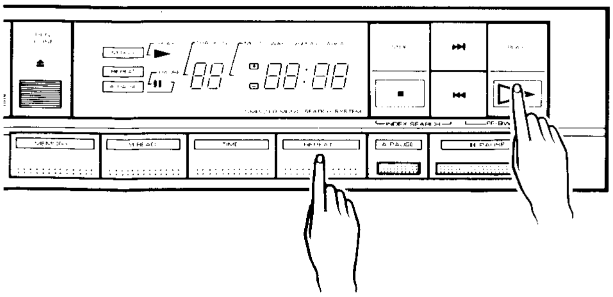
1. Select the track No. of the desired selection with the music search switches (⏮ ⏭). The track No. indicator (TRACK NO.) shows the selected track No. To select the index No., refer to "Index search" of Music search switches (⏮ ⏭) (6) on page 5 .
2. Press the pause switch (❚❚ PAUSE). The pause indicator lights and the unit enters the pause mode at the beginning of the selected tune.
3. To start playback, press the play switch (▷ PLAY). The play indicator (▶ PLAY) lights and the unit starts playing back the selected tune.

When the unit is set to pause mode, the unit enters the pause mode at the beginning of the selected tune and starts after step 1.



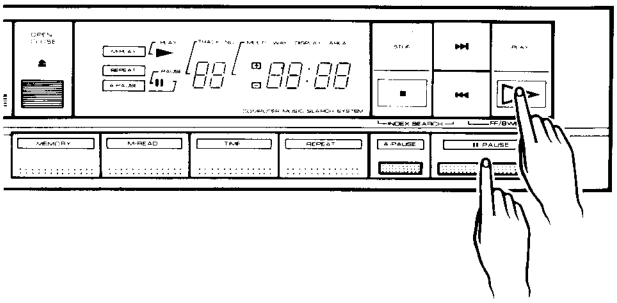
■ Full repeat playback

1. Press the play switch (▷ PLAY) and press the repeat switch (REPEAT). The repeat indicator (REPEAT) lights and all tunes are played back over again.
2. To release the full repeat playback mode, press the repeat switch (REPEAT) again. The repeat indicator (REPEAT) goes off and the laser pickup returns to the start position and the unit enters the standby mode after playing back the last tune.



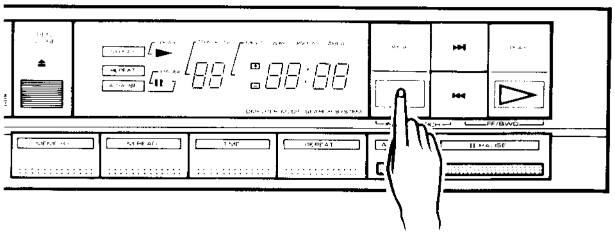
■ How to stop playback temporarily

1. To suspend playback, press the pause switch (❚❚ PAUSE). The pause indicator (❚❚ PAUSE) lights and the unit enters the pause mode.
2. To resume playback, press the play switch (▷ PLAY). The pause indicator (❚❚ PAUSE) goes off, the play indicator (▶ PLAY) lights and the playback starts.



■ How to enter standby mode

To stop playback and return the laser pickup to the beginning of the first tune, press the stop switch (■ STOP). The laser pickup returns to the start position and the unit enters the standby mode. The track No. indicator (TRACK NO.) displays 0 1.



Memory playback

■ How to memorize

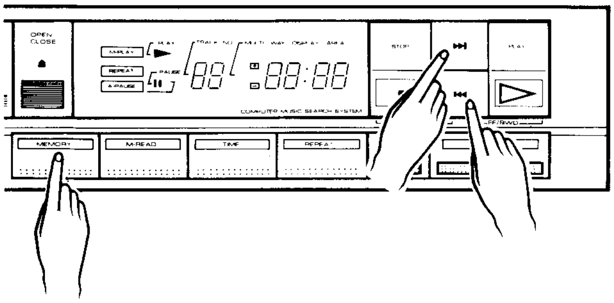
1. Press the power switch (POWER).
2. Place a disc on the disc tray.
3. When the mode display shows " 0 1 00:00 ", select the track No. of the desired selection with the music search switches (⏮ ⏭). The track No. indicator (TRACK NO.) shows the selected track No.
4. While the track No. indicator (TRACK NO.) shows the track No., press the memory switch (MEMORY). The MULTI WAY DISPLAY AREA shows the channel No.

1. FUNDAMENTALS OF OPERATION

5. To memorize the selection being played, press the memory switch (MEMORY) during play. The track No. indicator (TRACK NO.) shows the track No. of the selection being played and the MULTI WAY DISPLAY AREA shows the channel No.

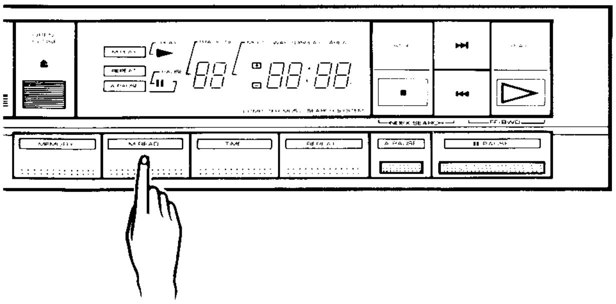
Notes:

1. Up to 16 selections can be memorized.
2. Memory is not possible in memory playback mode.



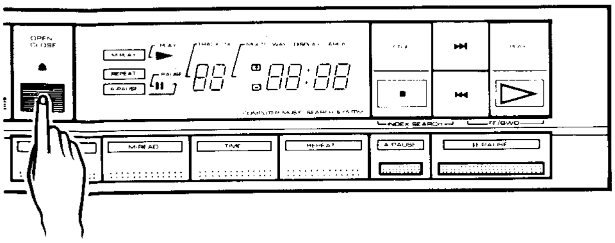
■ How to check the contents of memory

1. To check the memorized selection, press the memory read switch (M-READ). The track No. of the memorized selection is displayed in the track No. indicator (TRACK NO.). The MULTI WAY DISPLAY AREA shows the channel No.
2. Each time the memory read switch (M-READ) is pressed, the contents of the next memory can be checked.



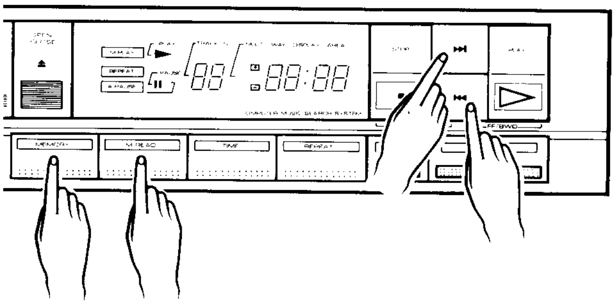
■ How to clear memorized selections

Press the open/close switch (▲ OPEN/CLOSE) to clear the memorized selections.



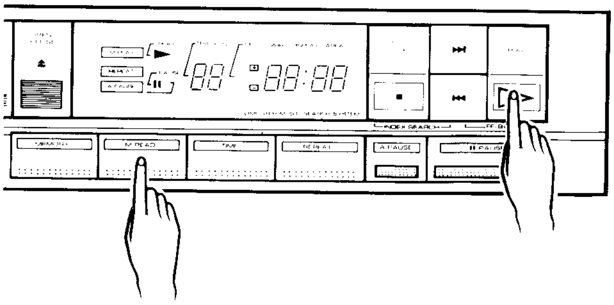
■ How to change the memory contents

1. Press the memory read switch (M-READ) to recall the memory channel to be changed.
2. Specify a new track number with the music search switches (⏮ ⏭).
3. Press the memory switch (MEMORY).



■ Memory play

1. Press the memory read switch (M-READ). The track No. and the channel No. of the selection memorized in channel 1 are displayed. To start memory play from halfway of the memorized selections, press the memory read switch (M-READ) repeatedly.
2. Press the play switch (▷ PLAY). The memory play indicator (M-PLAY) lights and play starts from the specified selection, providing a blank section of about 4 seconds between selections.
3. When the last tune of the number which is stored in memory is played back, the laser pickup returns to the beginning of the first tune and the unit enters the standby mode. The memory play mode is released.

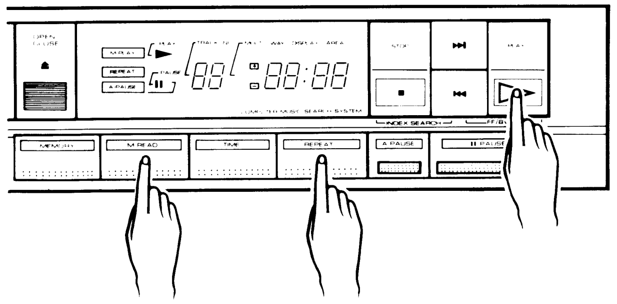


1. FUNDAMENTALS OF OPERATION

1-5. NOTES ON HANDLING COMPACT DISCS IN CASE OF DIFFICULTY

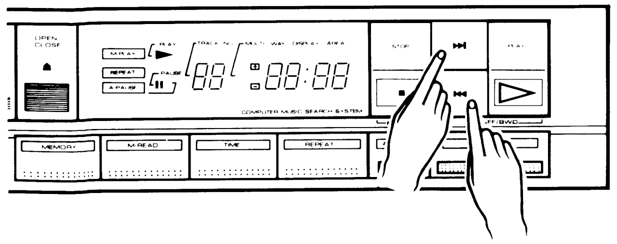
■ Memory repeat playback

1. Press the memory read switch (M-READ). The track No. and the channel No. of the selection memorized in channel 1 are displayed. To start play from halfway of the memorized selections, press the memory read switch (M-READ) repeatedly.
2. Press the play switch (▷ PLAY) and repeat switch (REPEAT). The memory play indicator (M-PLAY) and repeat indicator (REPEAT) light. The playback starts from the specified memory channel and all the tunes are played back.
3. To release memory repeat playback, press the repeat switch (REPEAT). The repeat indicator (REPEAT) goes off. When the last tune is played back, the laser pickup returns to the start position and the unit enters the standby mode. The memory play mode is released.
4. When one tune number is stored in memory and the unit is set to the repeat mode, repeat playback of one tune is possible.



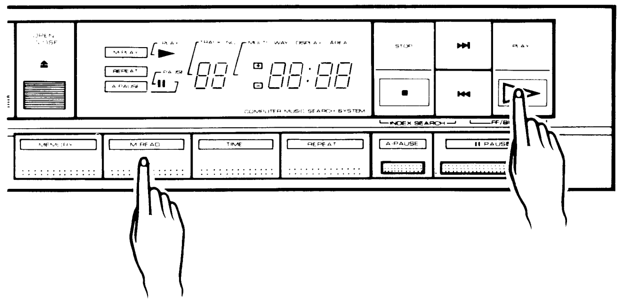
■ How to select the next or subsequent tunes during memory play

1. Press the music search switches (⏮, ⏭) during memory play. The track No. indicator (TRACK NO.) shows the No. of the next or subsequent tune, playback starts from the beginning of the next or subsequent tune.
2. By pressing the music search switches (⏮, ⏭) a number of times or continuously, any next or subsequent memorized tune can be selected and played back.



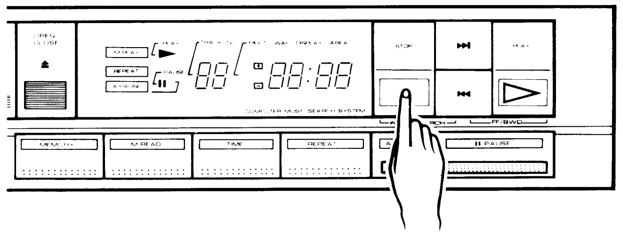
■ Memory play selection

1. Press the memory read switch (M-READ) during memory play to recall the desired tune No.
2. Press the play switch (▷ PLAY). Playback starts from the specified tune.



■ How to change from memory play to manual play

Press the stop switch (■ STOP). Playback stops, the laser pickup returns to its start position and the unit enters the standby mode. The memory play mode is released.



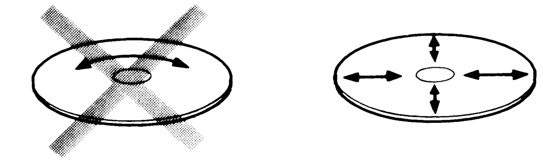
SPECIFICATIONS

Handling

Compact discs are made of plastic (polycarbonate). When the recorded side of the compact disc is dirty or scratched, playback may be noisy or sound may be missed. Even when the label side is scratched, the recording may be damaged. Handle compact discs carefully. Do not stick tape, etc. to compact discs.

Cleaning

When a compact disc is contaminated with fingerprints, etc., wipe with a dry cloth in a radial direction. Never use chemical solvents, such as thinner, benzene, etc. and conventional record cleaners or aerosols.



Storage

Always replace the compact disc in its case and store it. Compact discs are adversely affected by heat and moisture. Do not store compact discs in a place exposed to direct sunlight or where humidity is high.

Additional precautions

When performing connections, always disconnect the power cord from the AC outlet. When setting the power switch (POWER) to OFF, always turn the volume control of the amplifier to minimum.

1-6. DISASSEMBLY FOR REPAIR

Replacement of pickup.

When replacing the pickup, remove the ❸ screw (❶ ~ ❸) as shown below.

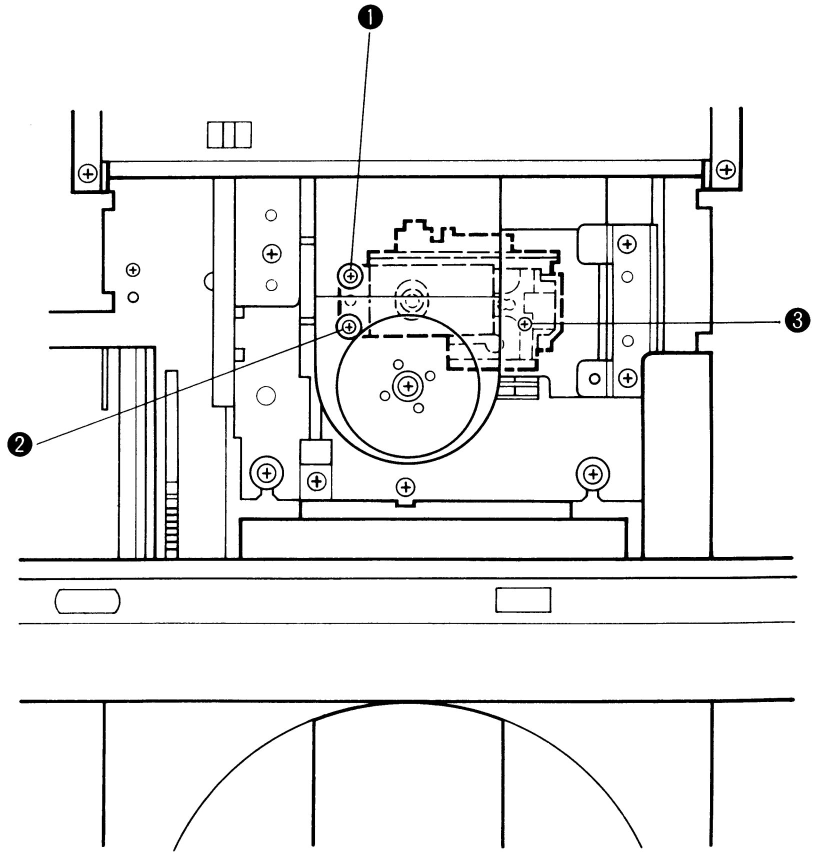
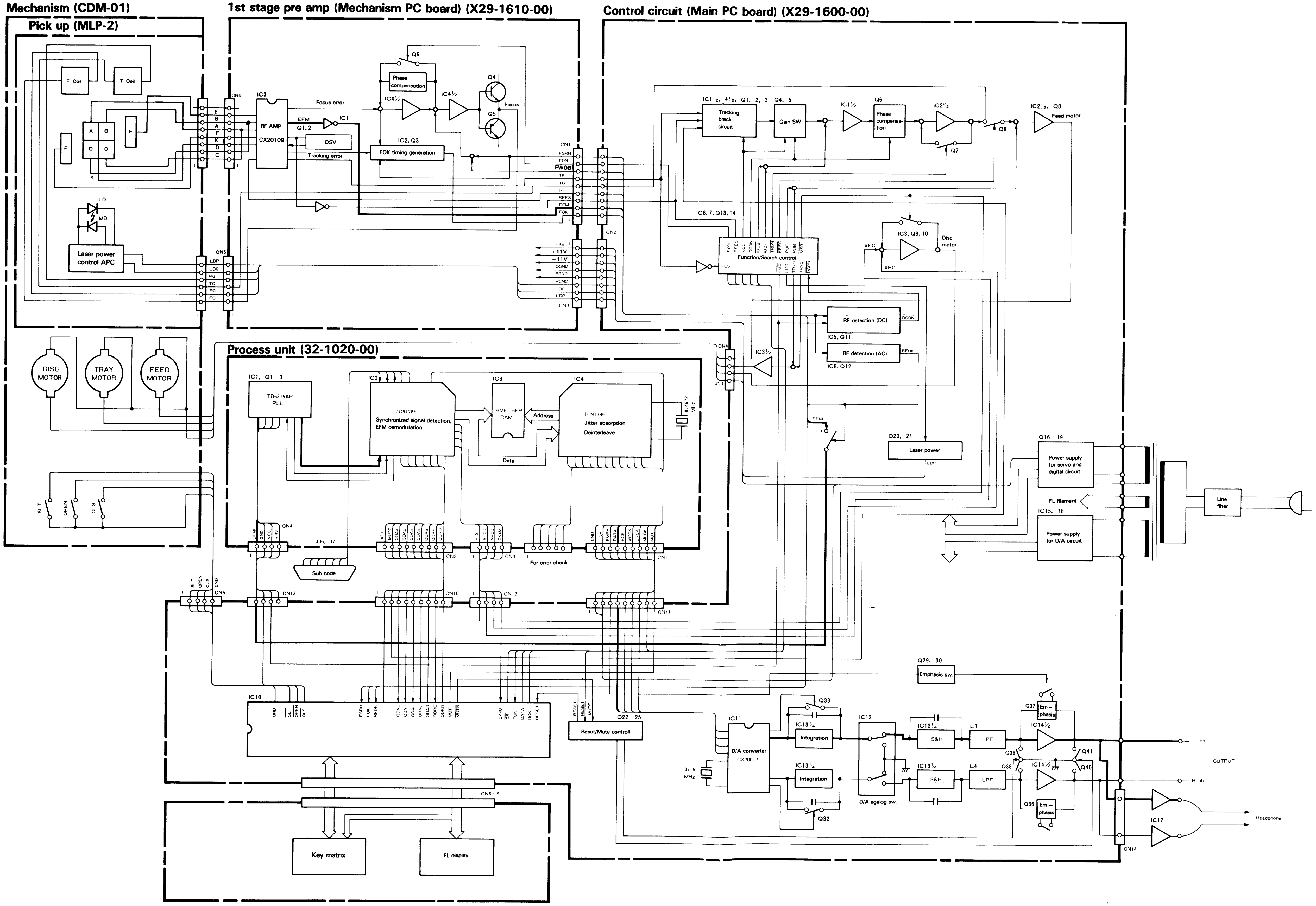


Fig. 1

2. BLOCK DIAGRAM


Mechanism (CDM-01)
Pick up (MLP-2)
F-Coil
T-Coil
A
B
C
D
E
F
K
LD
MD
Laser power control APC
DISC MOTOR
TRAY MOTOR
FEED MOTOR
SLT
OPEN
CLS
1st stage pre amp (Mechanism PC board) (X29-1610-00)
CN4
CN5
LDP
LDG
PG
TC
FC
IC3
RF AMP
CX20109
Focus error
EFM
IC1
Q1, 2
DSV
Tracking error
Q6
Phase compensation
IC4½
Q4
Q5
Focus
IC2, Q3
FOK timing generation
CN1
FSRH
FON
FWOB
TE
RF
RFES
FOK
CN2
-5V
+11V
-11V
DGND
SGND
PGND
CN3
Control circuit (Main PC board) (X29-1600-00)
IC1½, 4½, Q1, 2, 3
Q4, 5
Tracking brack circuit
Gain SW
IC1½
Phase compensa-tion
IC2⅔
IC2½, Q8
Feed motor
Q7
Q8
IC6, 7, Q13, 14
Function/Search control
TES
AFC
IC3, Q9, 10
Disc motor
APC
RF detection (DC)
DCON
IC5, Q11
RF detection (AC)
RFOK
IC8, Q12
IC3½
Q20, 21
Laser power
LDP
Q16 ~ 19
Power supply for servo and digital circuit.
FL filament
IC15, 16
Power supply for D/A circuit
Line filter
Process unit (32-1020-00)
IC1, Q1 ~ 3
TD6315AP
PLL
IC2
TC9178F
Synchronized signal detection, EFM demodulation
IC3
HM6116FP
RAM
Address
Data
IC4
TC9179F
Jitter absorption
Deinterleave
8.4672 MHz
J36, 37
Sub code
For error check
CN4
CN2
CN3
CN1
CN5
CN13
CN10
CN12
CN11
IC10
GND
SLT
OPEN
CLS
FSRH
FOK
RFOK
ATT
DATA
RESET
RESET
MUTE
Q22 ~ 25
Reset/Mute controll
CN6 ~ 9
Key matrix
FL display
Q29, 30
Emphasis sw.
IC11
D/A converter
CX20017
37.5 MHz
Q33
IC13¼
Integration
Q32
IC12
D/A agalog sw.
S&H
L3
L4
LPF
Q37
Em-phasis
Q36
IC14½
Q39
Q38
Q41
Q40
L ch
R ch
OUTPUT
IC17
Headphone
CN14

3. CIRCUIT DESCRIPTION

3-1 SEMICONDUCTOR FUNCTIONS

3-1-1 Control circuit unit (Mechanism PCB) (X29-1610-00)

Components	Functions	Operations (Substitutions)
IC3 CX20109	For CD RF amplifier	This is the first stage amplifier for the photo pickup output signal. It detects focus error and tracking error signals. It amplifies the RF signal and shapes the waveform of the signal (EFM signal). It detects the mirror signal (the signal to detect at inter-track spaces). It detects the focus OK signal (FOK).
IC1 TC40H004P	CMOS inverter EFM waveform shaper	This shapes the mirror signal waveform and drives Q1 and Q2. It also shapes the EFM signal waveform.
IC2 UPD4011BC	NAND gate	This generates the focus ON timing. (CMOS)
IC4 AN6555	Focus servo amplifier	This amplifies the focus servo system and compensates the frequency. (Dual OP amplifier)
Q1 2SC1815	Asymmetry controller	This fixes the asymmetry control level at dropout. (General purpose transistor (NPN)) (General purpose transistor (PNP))
Q2 2SA1015		
Q3 2SC1815	Focus servo	This judges the focus error signal level. (General purpose transistor (NPN))
Q4 2SD571	Focus servo	This used in the driver stage of the focus actuator. (Medium output transistor (NPN)) (Medium output transistor (PNP))
Q5 2SB514		
Q6 2SK301	Focus SW	This is the switch used to control ON and OFF of the focus servo. (General purpose FET)

* IC1 and IC3 are not interchangeable. Equivalent parts can be used for the other parts.

Table 3-1-1

3-1-2 Control circuit unit (Main PCB) (X29-1600-00)

Components	Functions	Operations
IC1 AN6555	Dual OP amplifier	This amplifies the tracking servo system. It generates the tracking brake pulse.
IC2 TA7256P	Dual power OP amplifier	This amplifies the tracking servo system and drives it. It amplifies the feed servo system and drives it.

Table 3-1-2

3. CIRCUIT DESCRIPTION

Components	Functions	Operations
IC3 TA7256P	Dual OP amplifier	This amplifies the disc motor servo system and drives it. Drives tray motor.
IC4 AN6555	Dual OP amplifier	This compares tracking error signals (TES). It converts the mirror signal level of the tracking brake circuit.
IC5 TA75393S	Dual comparator	This detects dropout and generates the dropout control pulse.
IC6 UPA80C	Transistor array	This converts the levels of each control signal.
IC7 TRD5010	CMOS gate array	This is used for the interface between the microprocessor and the servo system. It is also used as the kick operation controller.
IC8 TA75393S	Dual comparator	This detects the presence or absence of RF output.
IC9 TC40H000P	CMOS-NAND gate	This is the EFM signal gate (measure for disc actuation) and the inverter of each signal at the same time.
IC10 UPD7519G	Microprocessor	This accepts the key inputs, drives FL display and controls operations of the servo system, etc.
IC11 CX20017	D/A converter	
IC12 UPD4053BC	CMOS analog switch	This switches for L or R channels of the D/A converter output.
IC13 TL084CN	Quad FET input OP amplifier	This integrates the D/A converter output and holds samples.
IC14 NJM4560D	Dual OP amplifier	This amplifies the audio output and performs emphasis correction.
IC15 μPC78L12	Three-terminal regulator	This is used for regulating +12 V.
IC16 NJM79L12		This is used for regulating −12 V.
IC17 μPC4557C	Dual OP amplifier	This is used as the headphone amplifier.

Table 3-1-2

3. CIRCUIT DESCRIPTION

Components	Functions	Operations
Q1 2SK301	Tracking error signal ON/OFF switch	Brake operation ON/OFF.
Q2 2SK301		
Q3 2SC2878	Tracking brake pulse control switch	Brake operation ON/OFF.
Q4 2SC2878	Tracking error signal/tracking brake pulse ON/OFF control switch	Tracking servo open/close operation during search operation.
Q5 2SC2878	Tracking gain control switch for dropout control	
Q6 2SK301	Tracking servo phase compensation control switch for dropout control	
Q7 2SK301	Tracking servo ON/OFF control switch	
Q8 2SC2878	Feed motor ON/OFF control switch	
Q9 2SK301	Disc motor ON/OFF control switch	
Q10 2SC2878	Reversal prevention for disc motor	
Q11 2SC1815	Flaw detector. It generates (IC5) → DCON signal.	
Q12 2SC1815	RF detector. It judges whether or not (IC8) → ON TRACK.	
Q13 DTC144EFF	This is the control switch to continue the operation for a certain time even after the brake circuit is kicked. (Inhibits DCON)	
Q14 2SC1815	This controls the focus search signal (FSRH) by the laser diode lighting signal (LDC).	
Q15 2SA1015	This applies an appropriate hum to prevent the actuator from being caught in focus searching. (FWOB)	

Table 3-1-2

3. CIRCUIT DESCRIPTION

Components	Functions	Operations
Q16 2SB514	Regulated power supply	This forms the +5 V regulated power supply in a pair with Q18.
Q18 2SC1815		Used in a pair with Q16. (Inverted Darlington circuit)
Q17 2SD330	Regulated power supply	This forms the −5 V regulated power supply in a pair with Q19.
Q19 2SA1015		Used in a pair with Q17. (Inverted Darlington circuit)
Q20 2SA1015	Laser power ON/OFF controller	
Q21 2SB605	This is used for turning on the laser beam.	
Q22 2SA1015	Power ON. Reset circuit.	
Q23 2SA1015	This converts the mute signal level. Reset.	
Q24 2SC1815	This converts the mute signal level.	
Q25 2SC1815		
Q29 2SC1815	This inverts the emphasis signal.	
Q30 2SA1015	This converts the emphasis signal level.	
Q32, Q33 2SK152	D/A converter output charge/discharge switch.	
Q36, Q37 2SK246	This is used for deemphasis switching.	
Q38,Q39,Q40,Q41 2SC2878	This is used for mute switching.	

Table 3-1-2

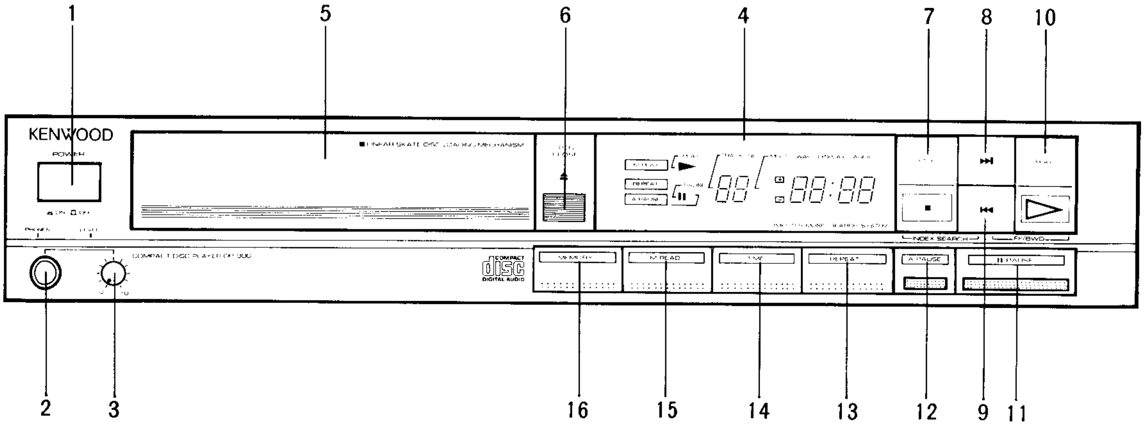
3. CIRCUIT DESCRIPTION

Components	Functions	Operations
Q28, Q31 2SK170	Constant-current circuit	
Q34, Q35 2SK246		
Q26, Q27 2SK246 (Y, G)		

Table 3-1-2

3-2 OUTLINE OF FUNCTIONS

The microprocessor IC10 (μPD7519G-167-36) was developed for the DP-900, and has the functions shown in Fig. 3-2.



1 to 3 are not related to the microprocessor.
4 to 16 are the functions related to the microprocessor.

Fig. 3-2

1. POWER switch
2. Headphone jack
3. Headphone volume
4. Display
5. Tray
6. OPEN/CLOSE key
7. STOP key
8. UP key
9. DOWN key
10. PLAY key
11. PAUSE key
12. A-PAUSE key
13. REPEAT key
14. TIME key
15. M-READ key
16. MEMORY key

STOP + UP......................................Index UP
STOP + DOWN ....Index DOWN
PLAY + UP......................................FF
PLAY + DOWN.................................FB

3. CIRCUIT DESCRIPTION

3-3 OUTLINE OF OPERATION

The microprocessor IC10 operates in six modes as shown in Fig. 3-3. The meaning of the key inputs are different in the test mode.

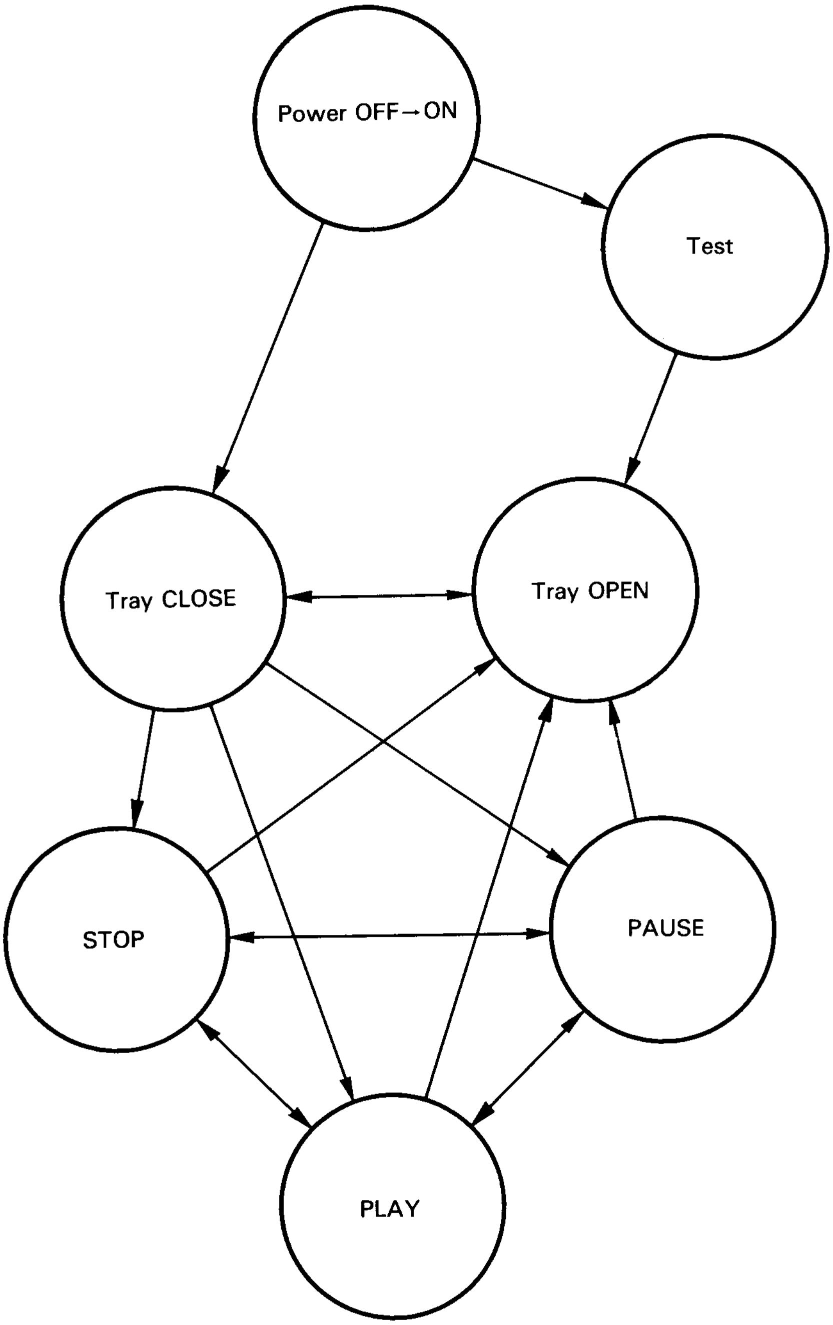

Power OFF→ON
Test
Tray CLOSE
Tray OPEN
STOP
PAUSE
PLAY

Fig. 3-3

3. CIRCUIT DESCRIPTION

3-3-1 TEST

When the PLST terminal (pin 16) of IC10 is "L" with the power ON, IC10 executes the transition of states as shown in Fig. 3-3-1.

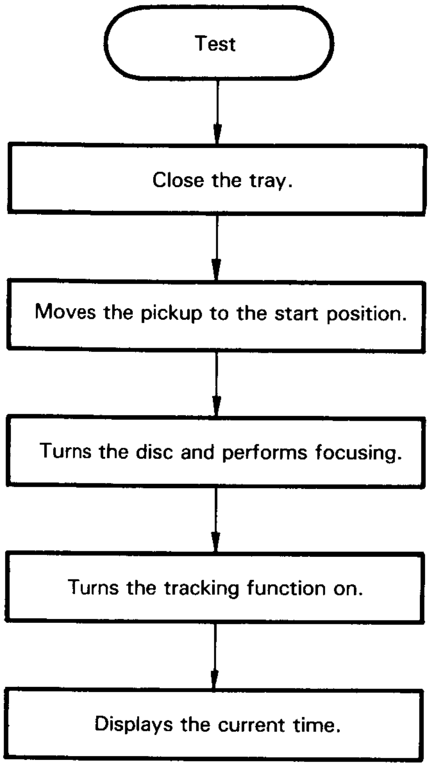

Test
Close the tray.
Moves the pickup to the start position.
Turns the disc and performs focusing.
Turns the tracking function on.
Displays the current time.

Fig. 3-3-1

3-3-2 Tray CLOSE

IC10 closes the tray and when a disc is set, IC10 reads the TOC (Table Of Contents).

3-3-3 Tray OPEN

IC10 opens the tray.

3-3-4 STOP

IC10 moves the pickup to the start position and turns the laser beam on. When the PLAY or PAUSE key is pressed, IC10 moves the operation mode to PLAY or PAUSE in the sequence shown in Fig. 3-3-2.

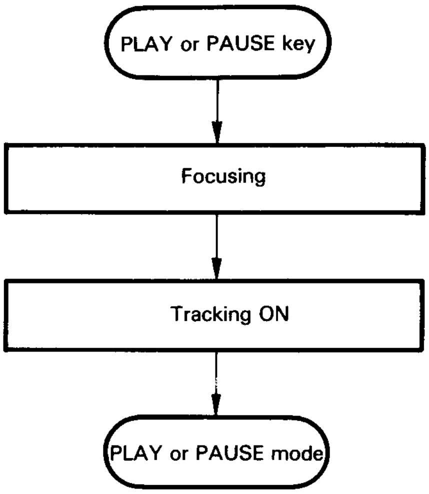

PLAY or PAUSE key
Focusing
Tracking ON
PLAY or PAUSE mode

Fig. 3-3-2

3-3-5 PAUSE

IC10 holds the pickup at the specified position as shown in Fig. 3-3-3.

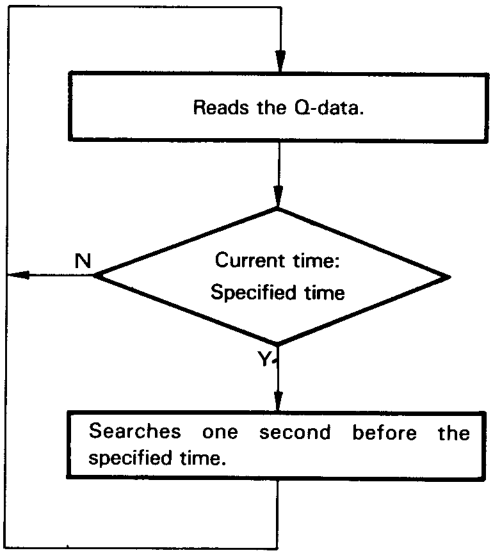

Reads the Q-data.
N
Current time:
Specified time
Y
Searches one second before the specified time.

Fig. 3-3-3

3-3-6 PLAY

IC10 turns MUTE off and displays the current time.

3. CIRCUIT DESCRIPTION

3-4 DESCRIPTION OF KEYS (See the page 17.)

Table 3-4-1 Test mode (PLST: L)

No.	Name	Function
6	OPEN/CLOSE	• This opens or closes the tray. • This clears the memory.
7	B1 (STOP)	This kicks 1 track backward.
8	UP	This kicks about 200 tracks forward.
9	DOWN	This kicks about 200 tracks backward.
10	TRON (PLAY)	Tracking ON (Pickup feed OFF)
11	FCON (PAUSE)	Focus ON (Tracking OFF, Pickup feed OFF)
12	F1 (A-PAUSE)	This kicks 1 track forward.
13	F3 (REPEAT)	This kicks 3 tracks forward.
14	F31 (TIME)	This kicks 31 tracks forward.
15	B3 (M-READ)	This kicks 3 tracks backward.
16	B31 (MEMORY)	This kicks 31 tracks backward.

Table 3-4-1

Table 3-4-2 Normal mode (PLST: H)

No.	Name	Function
5	Tray	When this is pressed at OPEN, the CLOSE mode is entered.
6	OPEN/CLOSE	• This opens or closes the tray. • This clears the memory. • This releases REPEAT and A-PAUSE.
7	STOP	• This releases the PAUSE or PLAY mode and sets the STOP mode. • This releases the memory PLAY mode.
8	UP	• This searches the next TNO in the normal PLAY or PAUSE mode. • This searches the next channel in the memory PLAY mode. • STOP mode 1) TNO is incremented every 0.3 secons. 2) When the UP key is pressed together with the STOP key, X is incremented every 0.3 seconds. • Press the UP key together with the PLAY key. 1) For the first time, five tracks are kicked forward. 2) Every 0.1 secons, 15 tracks are kicked forward.
9	DOWN	• At normal PLAY or PAUSE mode 1) Single pressing searches the beginning of the current tune. 2) Thereafter, the preceding TNO is searched. • At memory PLAY 1) Single pressing searches the beginning of the current tune. 2) Thereafter, the preceding channel is searched. • When the DOWN key is pressed together with PLAY key 1) For the first time, 7 tracks are kicked backward. 2) Every 0.1 seconds, 15 tracks are kicked backward. • STOP mode 1) Every 0.3 seconds TNO is decremented. 2) When the DOWN key is pressed together with the STOP key, X is decremented every 0.3 seconds.

Table 3-4-2

3. CIRCUIT DESCRIPTION

No.	Name	Function
10	PLAY	• Tray OPEN mode The tray is closed and the PLAY mode is set. • At M-READ mode The memory PLAY mode is set. • STOP or PAUSE mode The PLAY mode is set. • Tray CLOSE mode (with no disc) The tray is opened.
11	PAUSE	• Tray OPEN mode The tray is closed and the PAUSE mode is set. • At M-READ mode The PAUSE mode of memory PLAY is set. • STOP or PLAY mode The PAUSE mode is set. • Tray CLOSE mode (with no disc) The tray is opened.
12	A-PAUSE	• ON/OFF selector switch • At ON 1) One tune is played and then the PAUSE mode is set. No operation when the pickup is fed to the end by the FF function. 2) The STOP mode is set when the REPEAT key is not turned on at the end of the last tune.
13	REPEAT	• ON/OFF selector switch • At ON The first tune is played after all the tunes are played in the normal PLAY mode or the last tune is played in the memory PLAY mode.
14	TIME	• TIME display selector • STOP mode → Normal ↓ 00:00 + ↓ 00:00 − (Max. time) • PLAY or PAUSE mode → Normal ↓ (Relative time) + ↓ (Absolute time) − (Max. time-Absolute time) • MEMORY or M-READ mode → Normal ↓ (CH - No. display) + (Total time)
15	M-READ	• TNO, CH-No. or total time of 1CH - XCH (max. memorised channel) is displayed for 3 seconds. • M-READ → PLAY Memory PLAY • M-READ → UP/DOWN → MEMORY Reload the memory contents.
16	MEMORY	• Memorize TNO. (Reject during memory play mode.) • Max. 16 channels • M-READ → UP/DOWN → MEMORY Reload the memory contents. • While the MEMORY key is pressed, TNO, CH-No. or the total time is displayed.

Table 3-4-2

3. CIRCUIT DESCRIPTION

3-4-3 Key scanning

During key scanning, KD1 - KD3 are usually "H" as shown in Fig. 3-4-1. When no key is pressed, K0 - K3 are "L". For example, when the PLAY key is pressed now, K0 becomes "H" and K1 - K3 become "L" if KD1 - KD3 are "H".
KD1 - KD3 are set to "H" in sequence and the others to "L", thereby checking which key of the matrix is pressed.

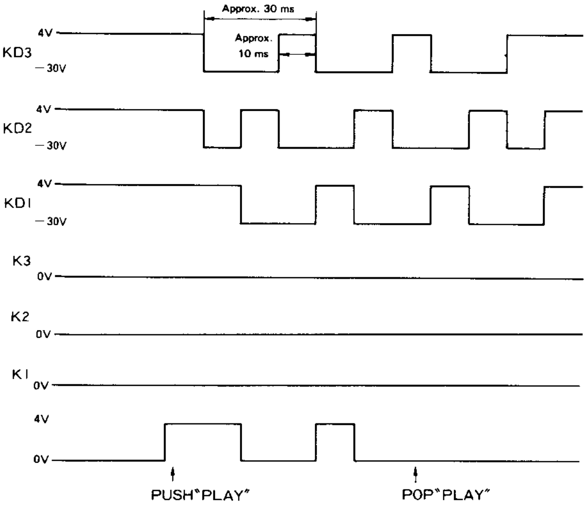

Approx. 30 ms
Approx. 10 ms
4V
KD3
−30V
4V
KD2
−30V
4V
KDI
−30V
K3
0V
K2
0V
KI
0V
4V
0V
PUSH"PLAY"
POP"PLAY"

Fig. 3-4-1

3-4-4 Display operation

The FL output waveform is as shown in Fig. 3-4-2.

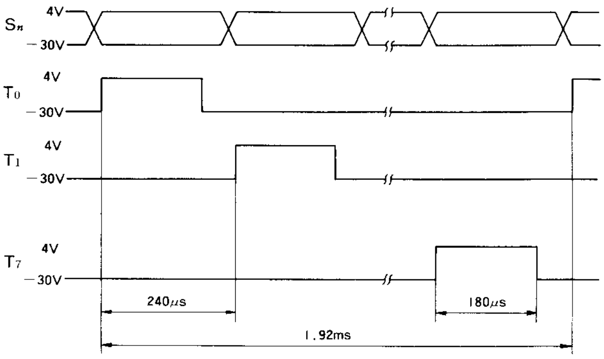

4V
S_n
−30V
4V
T_0
−30V
4V
T_1
−30V
4V
T_7
−30V
240μs
180μs
1.92ms

Fig. 3-4-2

3. CIRCUIT DESCRIPTION

3-4-5 Q-DATA reading

The Q-DATA is judged to have been read only when the conditions shown in Fig. 3-4-2 are met. Figs. 3-5-1, 3-5-2 and 3-5-3 show the timing of reading the Q-DATA.

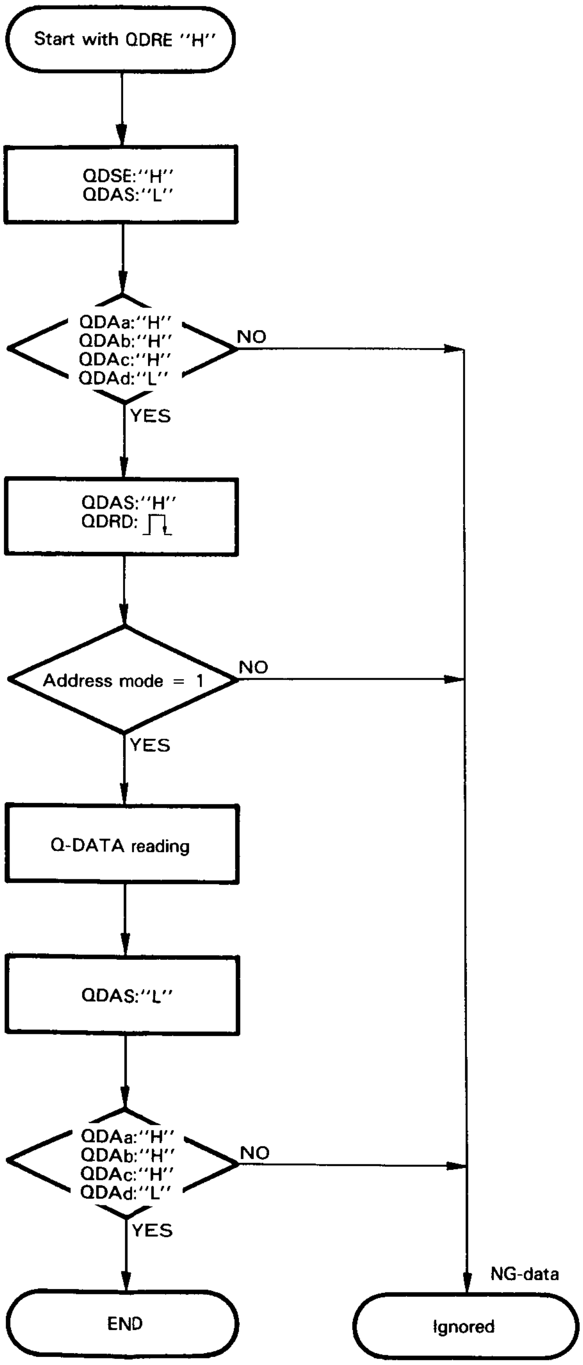

Start with QDRE "H"
QDSE:"H"
QDAS:"L"
QDAa:"H"
QDAb:"H"
QDAc:"H"
QDAd:"L"
NO
YES
QDAS:"H"
QDRD:
Address mode = 1
NO
YES
Q-DATA reading
QDAS:"L"
QDAa:"H"
QDAb:"H"
QDAc:"H"
QDAd:"L"
NO
YES
END
NG-data
Ignored

Fig. 3-4-3

3-4-6 Data transfer to TRD5010

The data is set at the trailing edge of DCK as shown in Fig. 3-4-4 for data transfer to TRD5010.

Therefore, the data is latched at the leading edge of DCK in TRD5010.

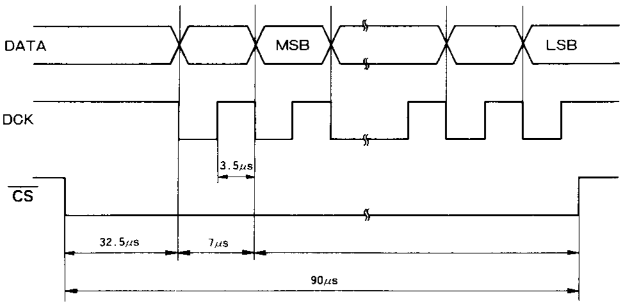

DATA
MSB
LSB
DCK
CS
3.5μs
32.5μs
7μs
90μs

Fig. 3-4-4

3. CIRCUIT DESCRIPTION

3-5 TIMING OF TEST MODE

(TRAY: OPEN, PU is set to the position with the SLT switch OFF, and the power ON.)

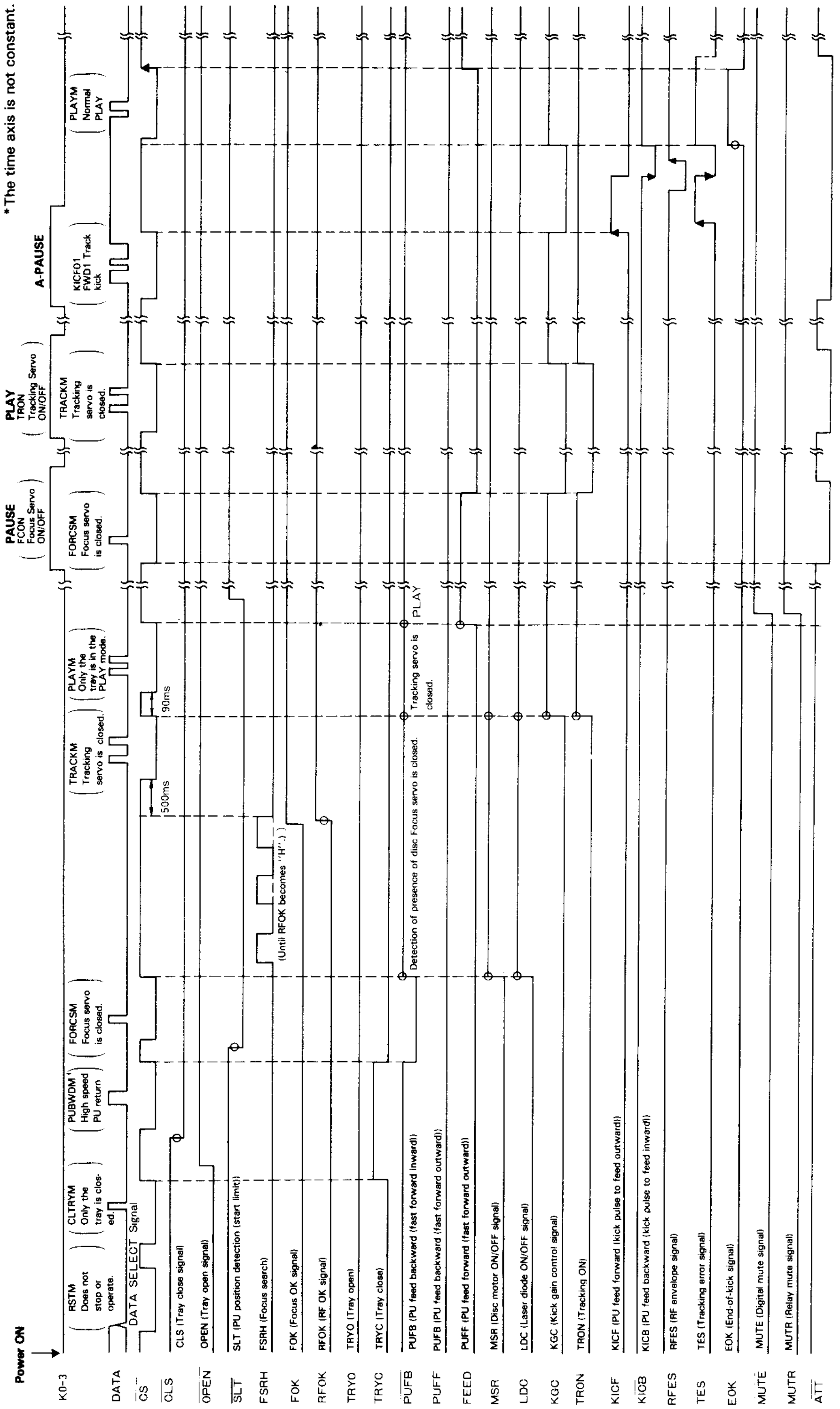

*The time axis is not constant.
Power ON
RSTM Does not stop or operate.
DATA SELECT Signal
CLTRYM Only the tray is closed.
PUBWDM High speed PU return
FORCSM Focus servo is closed.
(Until RFOK becomes "H".)
Detection of presence of disc Focus servo is closed.
500ms
TRACKM Tracking servo is closed.
90ms
PLAYM Only the tray is in the PLAY mode.
Tracking servo is closed.
PLAY
PAUSE FCON Focus Servo ON/OFF
FORCSM Focus servo is closed.
PLAY TRON Tracking Servo ON/OFF
TRACKM Tracking servo is closed.
A-PAUSE
KICF01 FWD1 Track kick
PLAYM Normal PLAY
K0-3
DATA
CS
CLS
OPEN
SLT
FSRH
FOK
RFOK
TRYO
TRYC
PUFB
PUFF
FEED
MSR
LDC
KGC
TRON
KICF
KICB
RFES
TES
EOK
MUTE
MUTR
ATT
CLS (Tray close signal)
OPEN (Tray open signal)
SLT (PU position detection (start limit))
FSRH (Focus search)
FOK (Focus OK signal)
RFOK (RF OK signal)
TRYO (Tray open)
TRYC (Tray close)
PUFB (PU feed backward (fast forward inward))
PUFB (PU feed backward (fast forward outward))
PUFF (PU feed forward (fast forward outward))
MSR (Disc motor ON/OFF signal)
LDC (Laser diode ON/OFF signal)
KGC (Kick gain control signal)
TRON (Tracking ON)
KICF (PU feed forward (kick pulse to feed outward))
KICB (PU feed backward (kick pulse to feed inward))
RFES (RF envelope signal)
TES (Tracking error signal)
EOK (End-of-kick signal)
MUTE (Digital mute signal)
MUTR (Relay mute signal)

Fig. 3-5-1

3. CIRCUIT DESCRIPTION

*The time axis is not constant.

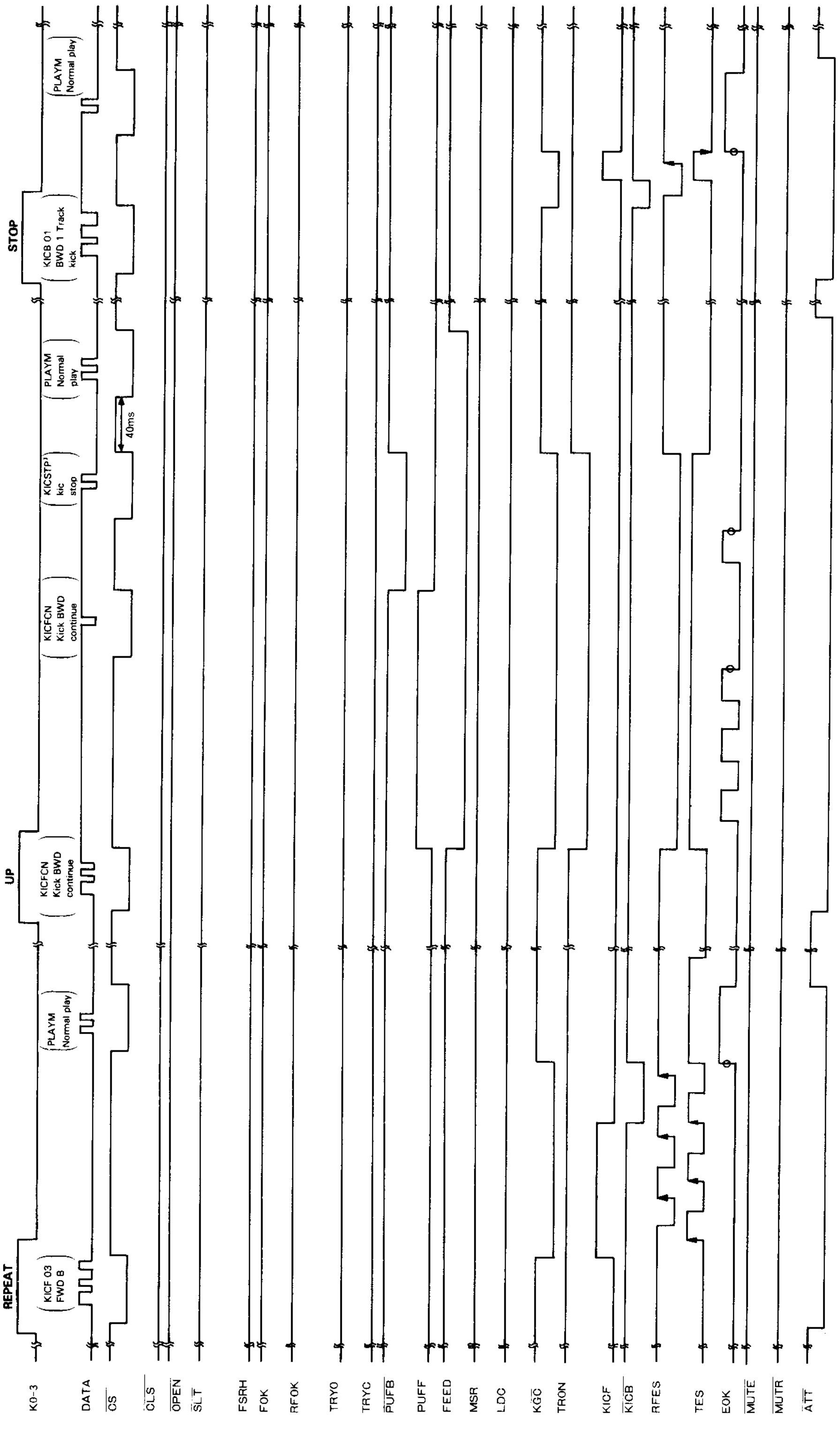
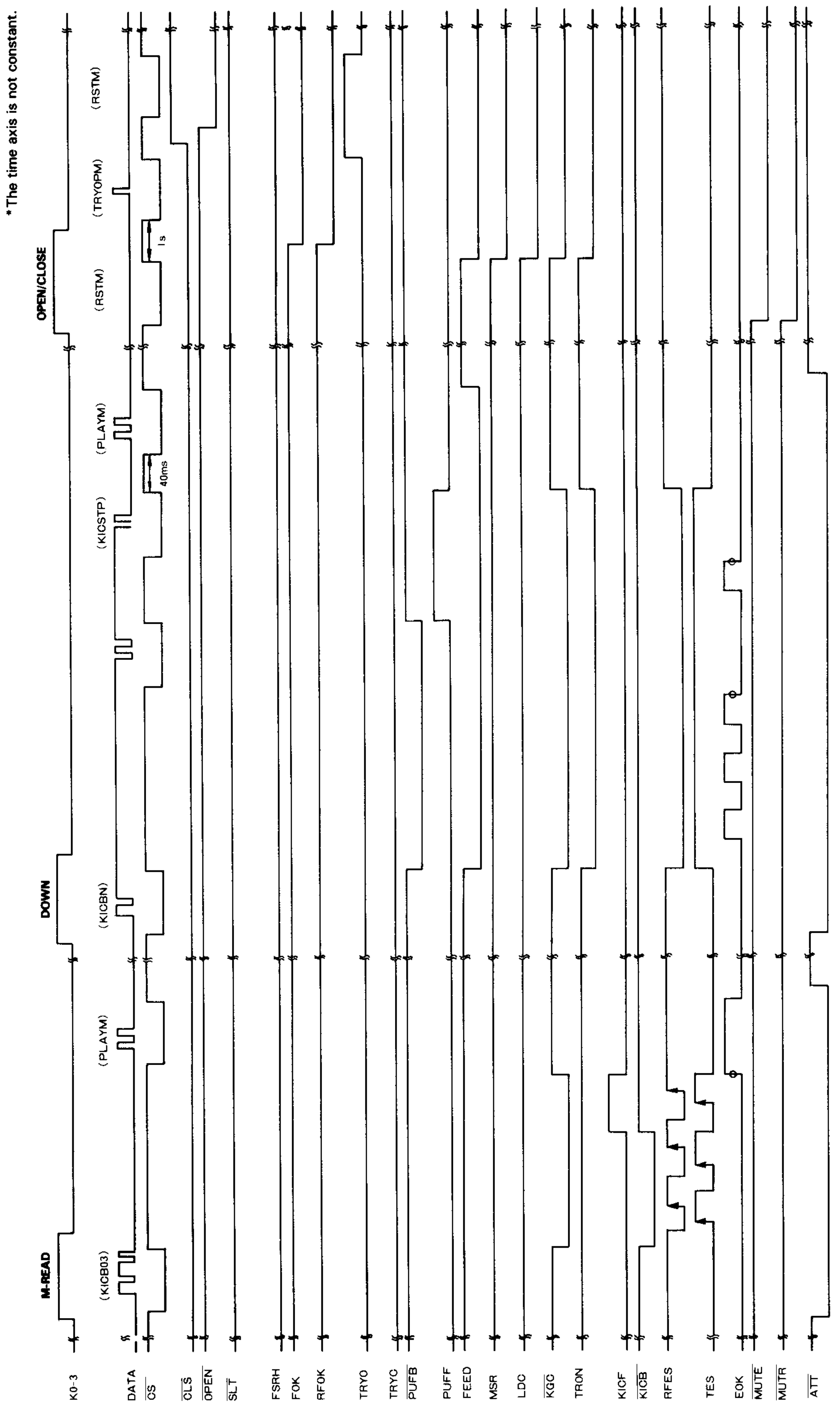

REPEAT
KICF 03 FWD 8
PLAYM Normal play
UP
KICFCN Kick BWD continue
KICFCN Kick BWD continue
KICSTP' kic stop
40ms
PLAYM Normal play
STOP
KICB 01 BWD 1 Track kick
PLAYM Normal play
K0-3
DATA
CS
CLS
OPEN
SLT
FSRH
FOK
RFOK
TRYO
TRYC
PUFB
PUFF
FEED
MSR
LDC
KGC
TRON
KICF
KICB
RFES
TES
EOK
MUTE
MUTR
ATT

Fig. 3-5-2

3. CIRCUIT DESCRIPTION


M-READ
DOWN
OPEN/CLOSE
(KICB03)
(PLAYM)
(KICBN)
(KICSTP)
40ms
(PLAYM)
(RSTM)
1s
(TRYOPM)
(RSTM)
K0-3
DATA
$\overline{\text{CS}}$
$\overline{\text{CLS}}$
$\overline{\text{OPEN}}$
$\overline{\text{SLT}}$
FSRH
FOK
RFOK
TRYO
TRYC
$\overline{\text{PUFB}}$
PUFF
FEED
MSR
LDC
$\overline{\text{KGC}}$
TRON
KICF
$\overline{\text{KICB}}$
RFES
TES
EOK
$\overline{\text{MUTE}}$
$\overline{\text{MUTR}}$
$\overline{\text{ATT}}$

*The time axis is not constant.

Fig. 3-5-3

3. CIRCUIT DESCRIPTION

3-6 FLOWCHART FROM POWER ON TO TIME DISPLAY IN TEST MODE (PLST: L)

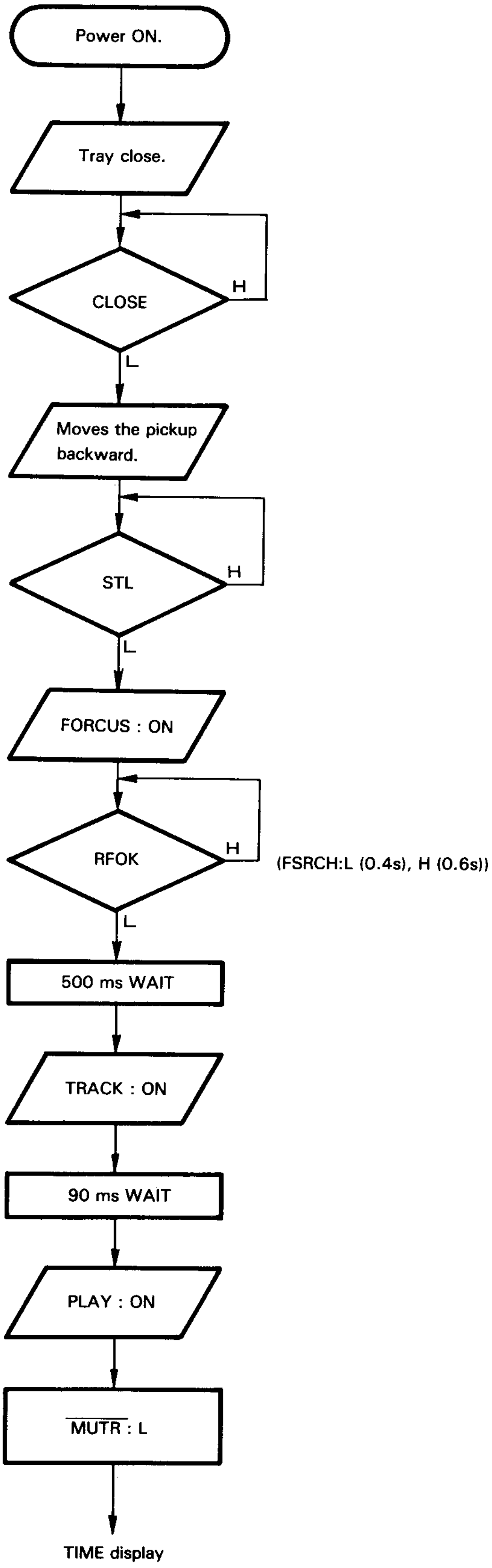

Power ON.
Tray close.
CLOSE
H
L
Moves the pickup backward.
STL
H
L
FORCUS : ON
RFOK
H
L
(FSRCH:L (0.4s), H (0.6s))
500 ms WAIT
TRACK : ON
90 ms WAIT
PLAY : ON
$\overline{\text{MUTR}}$: L
TIME display

Fig. 3-6-1

3. CIRCUIT DESCRIPTION

3-7 TIMING OF CLOSE STATE

(TRAY: OPEN, PU is set to the position with the SLT switch OFF and the power ON.)

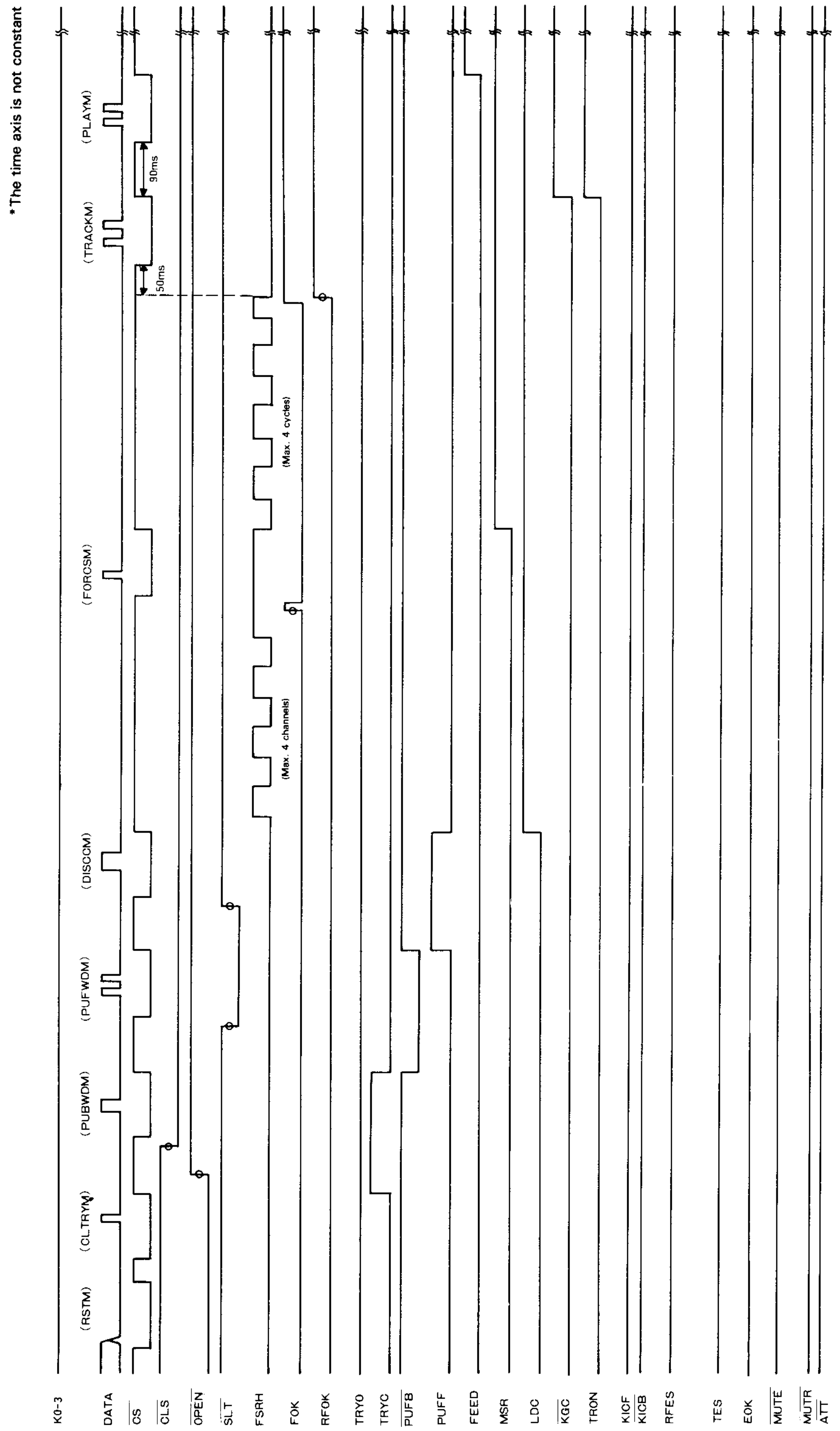

*The time axis is not constant
(RSTM)
(CLTRYM)
(PUBWDM)
(PUFWDM)
(DISCCM)
(FORCSM)
(TRACKM)
(PLAYM)
50ms
90ms
(Max. 4 channels)
(Max. 4 cycles)
K0-3
DATA
CS
CLS
OPEN
SLT
FSRH
FOK
RFOK
TRYO
TRYC
PUFB
PUFF
FEED
MSR
LDC
KGC
TRON
KICF
KICB
RFES
TES
EOK
MUTE
MUTR
ATT

Fig. 3-7-1

3. CIRCUIT DESCRIPTION

3-8 FLOWCHART FROM TRAY CLOSE TO TOC READING

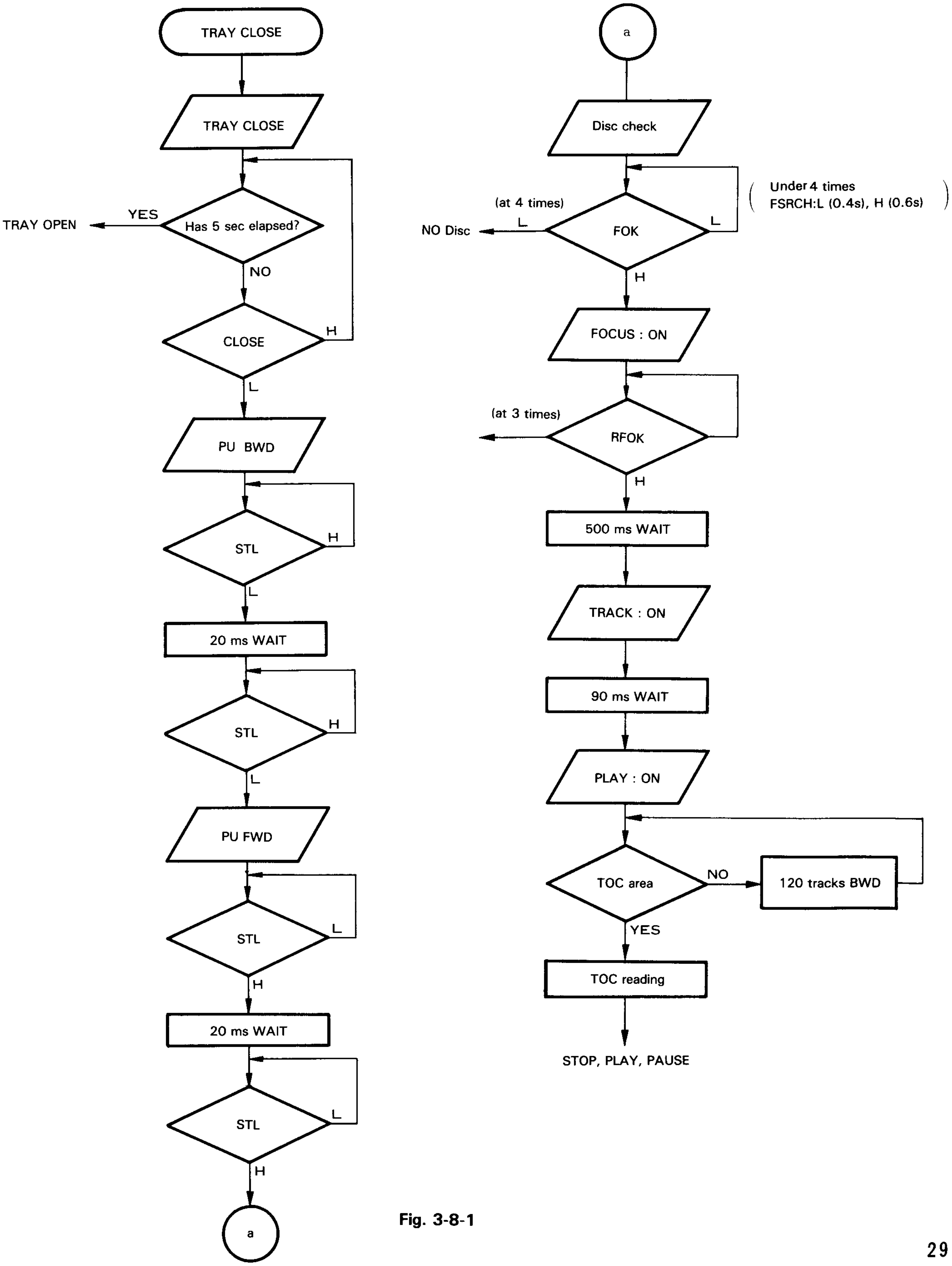

TRAY CLOSE
TRAY CLOSE
Has 5 sec elapsed?
YES
TRAY OPEN
NO
CLOSE
H
L
PU BWD
STL
H
L
20 ms WAIT
STL
H
L
PU FWD
STL
L
H
20 ms WAIT
STL
L
H
a
a
Disc check
FOK
(at 4 times)
L
NO Disc
L
Under 4 times
FSRCH:L (0.4s), H (0.6s)
H
FOCUS : ON
RFOK
(at 3 times)
H
500 ms WAIT
TRACK : ON
90 ms WAIT
PLAY : ON
TOC area
NO
120 tracks BWD
YES
TOC reading
STOP, PLAY, PAUSE

Fig. 3-8-1

3. CIRCUIT DESCRIPTION

3-9 DISPLAYS

Displays of the microprocessor IC10 are as shown in Fig. 3-9.

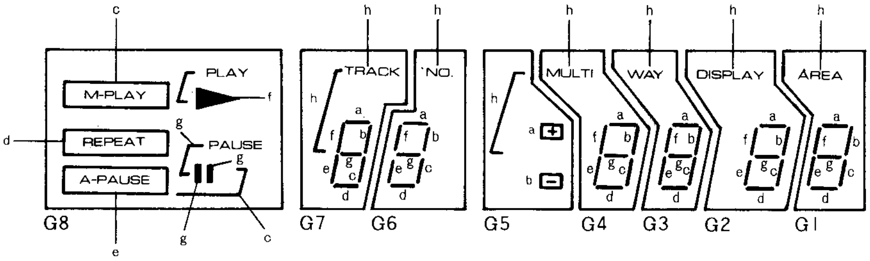


Fig. 3-9

3-9-1 Display contents

G	P	Name	Contents
8	c	M-PLAY	• This is lit during the M-PLAY mode. Lit when M-READ → PLAY. • Goes off when the STOP key is pressed.
8	d	REPEAT	• This is lit at REPEAT ON. • Turned on and off by the REPEAT key.
8	e	A-PAUSE	• This is lit at A-PAUSE ON. • Turned on and off by the A-PAUSE key.
8	f	PLAY	• This is lit during the PLAY mode or when the PLAY key is pressed. • During the interval (4 seconds) between tunes in the memory PLAY mode, it is lit although the mode is PAUSE.
8	g	PAUSE	• This is lit during the PAUSE mode or when the PAUSE key is pressed.
7 6		TNO	• The track No. is displayed. • The memory channel contents are displayed in MEMORY or M-READ mode.
5	a	+	• This is lit when the absolute time is displayed.
5	b	–	• This is lit when the remaining time is displayed.
4 ~ 1		Time display	• X display • CH display • Relative time display • Absolute time display • Remaining time display

Table 3-9-1

3. CIRCUIT DESCRIPTION

3-9-2. Display states

(1) Test

PLAY is lit and TNO being played and absolute time are displayed as shown in Fig. 3-9-1.

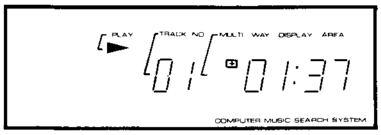

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
01
01:37
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-1

(2) OPEN

The display becomes as shown in Fig. 3-9-2 at the beginning of opening the tray and when the tray is opened.

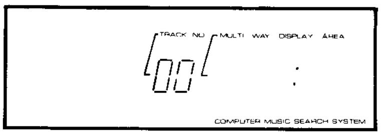

TRACK NO
MULTI WAY DISPLAY AREA
00
:
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-2

The display becomes as shown in Fig. 3-9-3 when the UP key is pressed once with the tray opened.

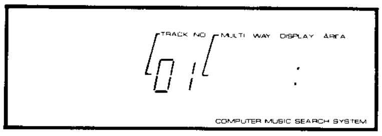

TRACK NO
MULTI WAY DISPLAY AREA
01
:
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-3

The display becomes as shown Fig. 3-9-4 when the UP (STOP + UP) of index is pressed once.

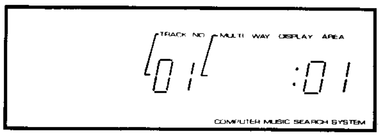

TRACK NO
MULTI WAY DISPLAY AREA
01
:01
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-4

(3) CLOSE

When the tray is pushed in the state shown in Fig. 3-9-4, the tray is closed, but the display is not changed from that shown in Fig. 3-9-4.

When the tray is closed by pressing the PLAY key, PLAY is displayed. PAUSE is displayed when the tray is closed by pressing the PAUSE key. After the tray is closed, the display becomes as shown in Fig. 3-9-5 if no disc is set.

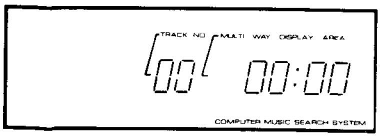

TRACK NO
MULTI WAY DISPLAY AREA
00
00:00
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-5

(4) STOP

TNO displays the minimum tune of the disc and the time is displayed as 00:00 as shown in Fig. 3-9-6.

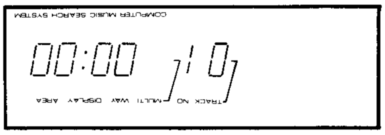

COMPUTER MUSIC SEARCH SYSTEM
TRACK NO
MULTI WAY DISPLAY AREA

Fig. 3-9-6

When the remaining time is displayed by pressing the TIME key twice, the disc end time is displayed as shown in Fig. 3-9-7.

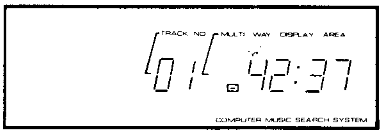

TRACK NO
MULTI WAY DISPLAY AREA
01
42:37
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-7

When TNO No. 3 is stored in the channel 1 by pressing the UP key, 3 is displayed for TNO and CH01 for the time display as shown in Fig. 3-9-8.

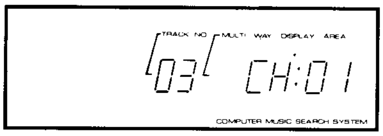

TRACK NO
MULTI WAY DISPLAY AREA
03
CH:01
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-8

When the TIME key is pressed then, the total time up to the channel stored now is displayed as shown Fig. 3-9-9.

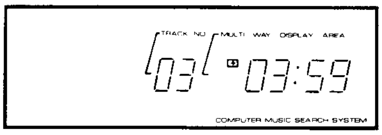

TRACK NO
MULTI WAY DISPLAY AREA
03
03:59
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-9

To change the contents of channel 1 from 3 to 4, operate in the order M-READ → UP → MEMORY. Then, the display is changed from Fig. 3-9-10 to Fig. 3-9-11 and Fig. 3-9-12.

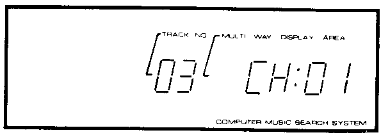

TRACK NO
MULTI WAY DISPLAY AREA
03
CH:01
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-10

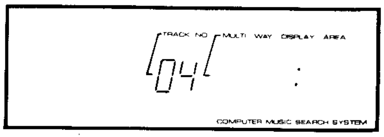

TRACK NO
MULTI WAY DISPLAY AREA
04
:
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-11

3. CIRCUIT DESCRIPTION

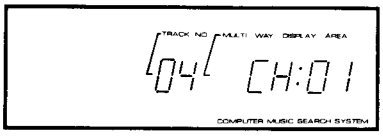

TRACK NO
MULTI WAY DISPLAY AREA
04
CH:01
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-12

(5) PLAY

While TNO No. 3 is being searched, the display becomes as shown in Fig. 3-9-13. When the searching operation ends, the display becomes as shown in Fig. 3-9-14.
While channel 1 is being searched, the display becomes as shown in Fig. 3-9-15. When the searching operation ends, the display becomes as shown in Fig. 3-9-16 and is held for 4 seconds and then the time will rise as in the normal PLAY mode. This is because a blank of 4 seconds is left at the beginning of each tune in the memory PLAY mode.

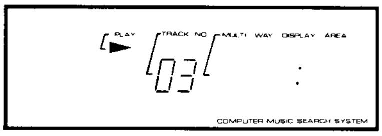

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
:
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-13

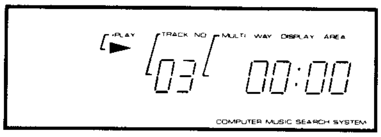

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
00:00
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-14

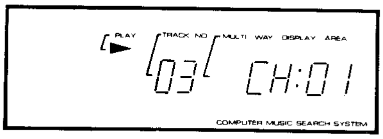

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
CH:01
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-15

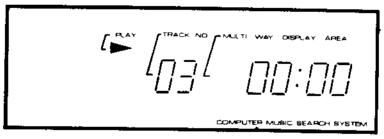

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
00:00
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-16

When the TIME key is pressed in the PLAY mode, the total time is displayed as shown in Fig. 3-9-18. The remaining time is displayed as shown in Fig. 3-9-19 when the TIME key is pressed once more. The relative time is displayed as shown in Fig. 3-9-17 when the TIME key is pressed one more time.

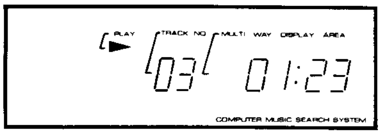

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
01:23
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-17

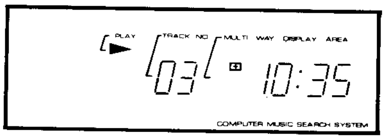

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
10:35
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-18

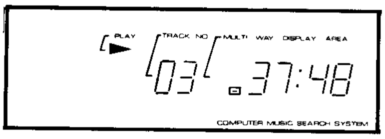

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
37:48
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-19

When the total time or remaining time is displayed as "—:—" as shown in Figs. 3-9-20 and 3-9-21 during the memory PLAY mode, it means that the total time of the memory exceeds 99 minutes 99 seconds or a TNO after No. 21 is stored (for example, a TNO number greater than 21 is stored for a disc in which the TNO begins with 1, and a TNO number greater than 24 is stored for a disc in which the TNO begins with 4).

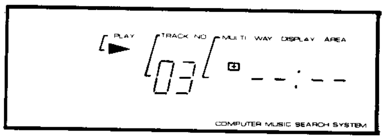

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
--:--
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-20

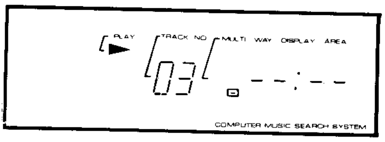

PLAY
TRACK NO
MULTI WAY DISPLAY AREA
03
--:--
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-21

(6) PAUSE

The PLAY display in the PLAY mode is changed to PAUSE as shown in Fig. 3-9-22. Fig. 3-9-22

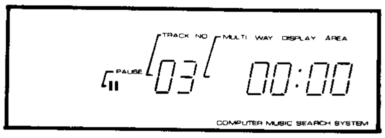

TRACK NO
MULTI WAY DISPLAY AREA
PAUSE
03
00:00
COMPUTER MUSIC SEARCH SYSTEM

Fig. 3-9-22

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-1 RF AMP: IC13 (CX20109)

The CX20109 is the bipolar IC that incorporates an RF amp for the output of a 3-spot type optical pickup developed for the compact disc player, as well as focus, mirror, trackng, EFM comparator, and other signal processing circuit required for controlling the system.

Pin connections

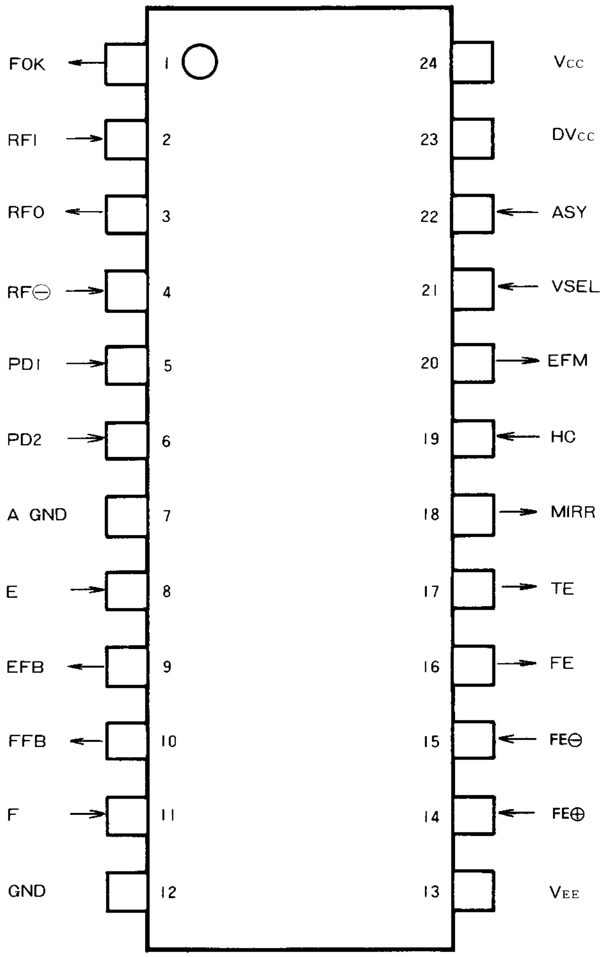

FOK
RFI
RFO
RF⊖
PD1
PD2
A GND
E
EFB
FFB
F
GND
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13
Vcc
DVcc
ASY
VSEL
EFM
HC
MIRR
TE
FE
FE⊖
FE⊕
VEE

Fig. 4-1-1
(Top view)

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Block diagram

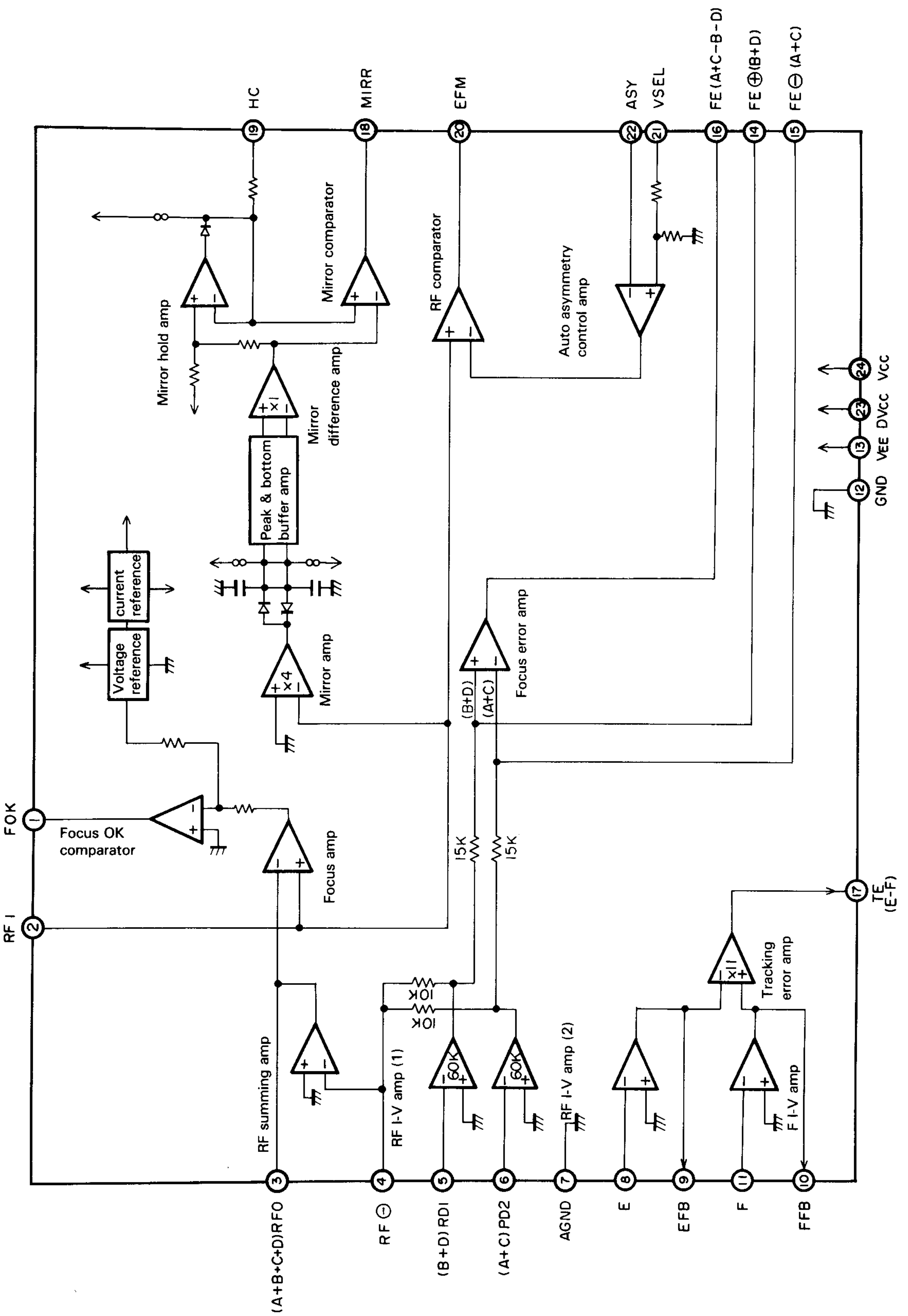

HC
MIRR
EFM
ASY
VSEL
FE (A+C−B−D)
FE ⊕(B+D)
FE ⊖ (A+C)
19
18
20
22
21
16
14
15
Mirror comparator
RF comparator
Auto asymmetry control amp
Mirror hold amp
Mirror difference amp
×1
Peak & bottom buffer amp
current reference
Voltage reference
Mirror amp
×4
Focus error amp
(B+D)
(A+C)
15K
15K
24 Vcc
23 DVcc
13 VEE
12 GND
FOK
1
Focus OK comparator
Focus amp
RF I
2
TE (E-F)
17
Tracking error amp
×11
10K
10K
60K
60K
RF summing amp
RF I-V amp (1)
RF I-V amp (2)
F I-V amp
3
4
5
6
7
8
9
11
10
(A+B+C+D)RFO
RF ⊖
(B+D)RDI
(A+C)PD2
AGND
E
EFB
F
FFB

Fig. 4-1-2

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description

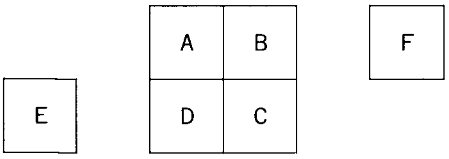
Pin number	Symbol	I/O	Function	DC Volt
1	FOK	O	Output of focusing servo allowed. Active at comparator output "H". Connects load resistor (PNP open collector).	0 V
2	RF1	I	Inputs RF summing amp output by a C coupling.	0 V
3	RFO	O	RF summing amp output. Eye pattern test point.	V_{RFO}
4	RF ⊖	I	RF summing amp inverted input. Connects feedback CR to ③ – ④.	0 V
5	PD 1	I	RF I-V amp (1) inverted input. Current input by connection to PIN diodes B + D.	0 V
6	PD 2	I	RF I-V amp (2) inverted input. Current input by connection to PIN diodes A + C.	0 V
7	AGND	–	Small signal analog channel ground	0 V
8	E	I	E I-V amp inverted input. Current input by connection to PIN diode E.	0 V
9	EFB	O	E I-V amp output connects feedback CR to ⑧ – ⑨.	0 V
10	FEB	0	F I-V amp output connects feedback CR to ⑩ – ⑪.	0 V
11	F	I	F I-V amp inverted input. Current input by connection to PIN diode F.	0 V
12	GND	–	GND	0 V
13	V_{EE}	–	Negative power supply	–5 V
14	FE ⊕	I	Focus error amp non-inverted input. Connects CR for low-pass filter.	0 V
15	FE ⊖	I	Focus error amp inverted input	0 V
16	FE	O	Focus error amp output. Connects feedback CR to ⑮ – ⑯.	V_{FEO}
17	TE	O	Tracking error amp output	V_{TEO}
18	MIRR	O	Mirror comparator output (active at "H"). Connects load resistor (PNP open collector).	0 V
19	HC	I	Mirror hold capacitor connecting pin	–2 V
20	EFM	O	EFM comparator output	4.1 V (OPEN)
21	VSEL	I	Auto-asymmetry control amp reference input level setting pin; V_{CC} when under ±5 V power supply. GND when under +10 V power supply.	+5 V
22	ASY	I	Auto-asymmetry control input	–
23	DV_{CC}	–	Positive power supply for EFM comparator	+5 V
24	V_{CC}	–	Positive power supply	+5 V

* Except for 20 , all DC potentials have been based on the standard test circuit.

Table 4-1-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Description of Operations



1. RF Amp

The PIN diode current inputs to PD1 And PD2 will be I-V converted by the individually 60 kΩ equivalent input resistance of RF I-V Amps (1) and (2). the converted outputs will then be summed together by the RF summing amp, and (A+B+C+D) output to RFO.
The pin will enable eye pattern checks.

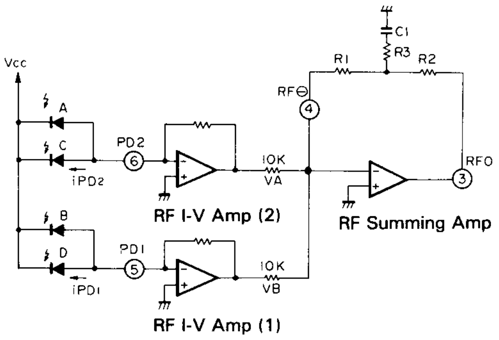

Vcc
A
C
PD2
6
iPD2
B
D
PD1
5
iPD1
RF I-V Amp (2)
RF I-V Amp (1)
10K
VA
10K
VB
C1
R1
R3
R2
RF⊖
4
RFO
3
RF Summing Amp

Fig. 4-1-3 RF I-V amp (1)

2. Focus Error Amp

This amp subtracts output (B+D) of the RF I-V amp (1) from output (A+C) of the RF I-V amp (2), And will output (A+C)−(B+D).

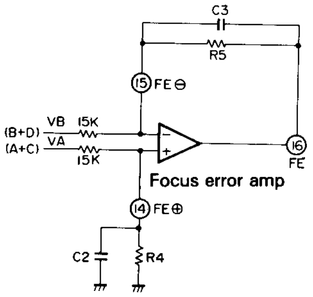

C3
R5
15 FE⊖
(B+D)
(A+C)
VB 15K
VA
15K
16
FE
Focus error amp
14 FE⊕
C2
R4

Fig. 4-1-4

C2 and C3 will be required for preventing the leakage of EFM components into the focus error output.

3. Tracking Error Amp

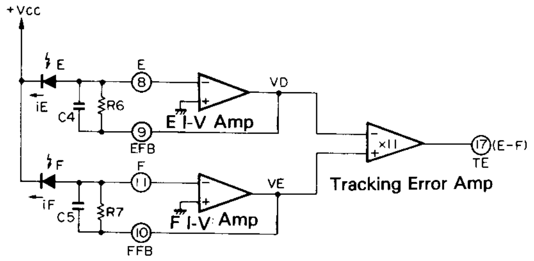

+Vcc
E
iE
C4
R6
E
8
E I-V Amp
9
EFB
VD
F
iF
C5
R7
F
11
F I-V Amp
10
FFB
VE
×11
17 (E-F)
TE
Tracking Error Amp

Fig. 4-1-5

The side spot PIN diode surrents that have been input to E and F will be I-V converted by the E and F I-V Amps at R6 and R7 respectively. Specifically:

$V_D = {}_{iE}R_6$
$V_E = {}_{iF}R_7$

In addition, the tracking error amp will take the difference of the E and F I-V amp outputs, and provide output (E-F). Because the tracking amp gain is 11 (21 dB), the following will hold:

$$V_{TE} = (V_D - V_E) \times 11$$
$$= (iE - iF) \times R_6 \times 11 \quad (R_6 = R_7)$$

C4 and C5 will be required for preventing the leakage of EFM components into the tracking error output.

4. Focus OK Circuit

The focus OK circuit serves the purpose of generating a window for the timing to turn the focusing servo on out of a focusing search mode.

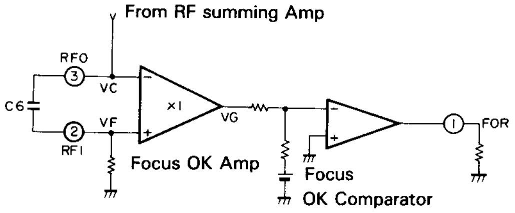

From RF summing Amp
RFO
3
VC
C6
2
VF
RFI
×1
VG
Focus OK Amp
Focus
OK Comparator
1
FOR

Fig. 4-1-6

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Becuase threshold level V_{TH} of the focus OK comparator has been arranged for inversion at $V_G = -0.4$ V, the focus OK comparator will invert itself when:

$V_{RFO} = V_C = 0.4$ V.

C6 dicates time constans of HPF in the EFM comparator, mirror circuit and LPF in the focus OK amp, and normally the selection of C6 = 0.01 μF that results in fc = 1.5 kHz will prevent the block error rate deterioration due to dropouts in the RF envelope caused by scratches and other defects in the disc.

5. Mirror Circuit

After amplifying the RFI signal, this circuit will perform its peak and bottom hold. The peak hold will be at a time constant that enables following up to as high as 30 kHz of traversing, while the bottom hold will be at another that enables following even the rotary frequency envelope fluctuations.

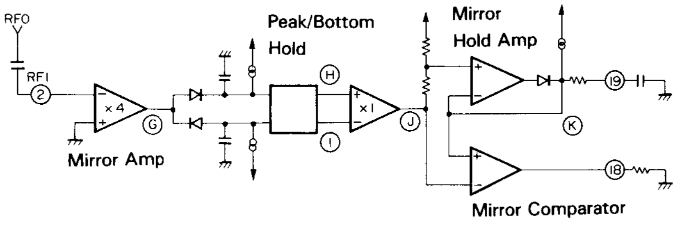


Fig. 4-1-7

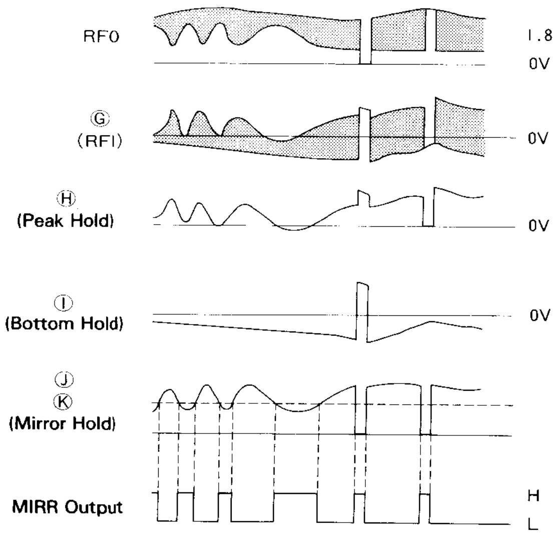


Fig. 4-1-8

By differential amplifying these peak/bottom hold signals, Ⓗ and Ⓘ DC restored envelope signal Ⓙ will be obtained. Mirror outputs may be obtained by comparing this Ⓙ signal with signal Ⓚ that has peak held the 2/3 level of peaks with a large time constant. Specifically, the mirror output will be at "L" when on tracks of the disc, at "H" when at inter-track spaces (mirror areas), and at "H" again when disc defects have been detected.

6. EFM Comparator

The EFM comparator serves for converting RF signals into binary codes. Since the asymmetry generated by deviations in the disc manufacture cannot be eliminated by AC couplings alone, control is exercised over the EFM comparator reference voltage through the utilization of 50% generating probabilities of "1" and "0" in the binary EFM signal.

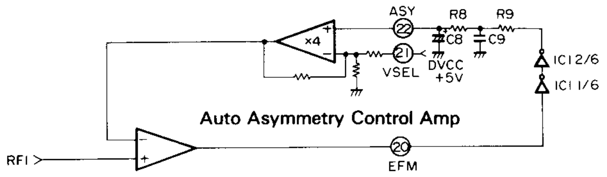


Fig. 4-1-9

R8, R9, C8 and C9 form an LPF to provide +2.5 V DC, and when its fc is made above 500 Hz, excessive leakage of low frequency components of EFM will result, deteriorating the block error rate.

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-2 KICK CONTROL: IC7 (TRD-5010)

Pin connection

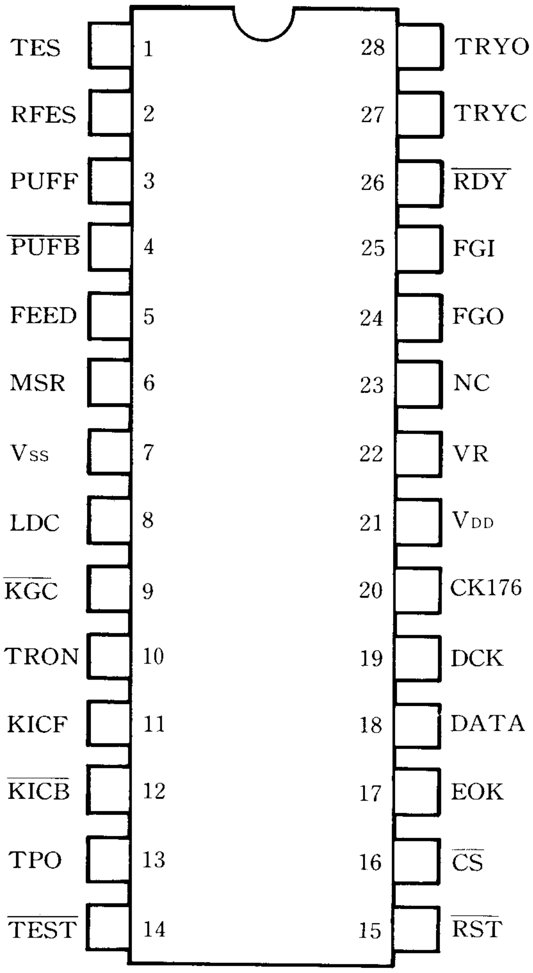

TES
1
RFES
2
PUFF
3
$\overline{PUFB}$
4
FEED
5
MSR
6
V_{SS}
7
LDC
8
$\overline{KGC}$
9
TRON
10
KICF
11
$\overline{KICB}$
12
TPO
13
$\overline{TEST}$
14
TRYO
28
TRYC
27
$\overline{RDY}$
26
FGI
25
FGO
24
NC
23
VR
22
V_{DD}
21
CK176
20
DCK
19
DATA
18
EOK
17
$\overline{CS}$
16
$\overline{RST}$
15

Fig. 4-2-1
(Top view)

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description

* In the DP-900, TPO = "L" : T/R = "L".

Pin No.	Name	I/O	Function
6	MSR	O	This turns on and off the disc motor. It works at the "H" level and stops at the "L" level by instructions from the microprocessor (IC10).
2	RFES	I	RF envelope detection input terminal. Counter enable signal to determine the kick amount, clock signal of more than 32 tracks to kick and the trailing edge (¯↓_⌈¯) of the counter enable signal.
1	TES	I	Tracking error signal input terminal. A clock of the counter to determine the kick amount. Counted at the trailing edge (_⌈¯↓_) of the input signal.
14	TEST	I	Semicustom test signal terminal. This is usually used at the "H" level. At the "L" level, it makes the play operation signal status regardless of input data. By setting this terminal to "L" level, the forced play mode is set in troubleshooting.
8	LDC	O	This turns on and off the laser diode. It lights the laser at the "H" level and turns it off at the "L" level. It is operated by instructions from the microprocessor (IC10).
18	DATA	I	Input terminal of 8-bit serial data from microprocessor (IC10). Control and data of kick direction and amount.
7	V_{ss}	I	GND
*22	T/R	I	TES/RFES clock signal selector. At the "L" level, the counter is clocked in TES for the kick of less than 31 tracks and RFES for that of more than 32 tracks. At the "H" level, all become TES.
20	CK176	I	176 kHz pulse input terminal. Clock used for internal operation.
28	TRYO	O	TRAY OPEN instruction terminal. Executed by the instruction from the microprocessor (IC10). This works at the "H" level and stops at the "L" level.
27	TRYC	O	TRAY CLOSE instruction terminal. Executed by the instruction from the microprocessor (IC10). This works at the "H" level and stops at the "L" level.
15	$\overline{RST}$	I	Terminal to reset the contents of 8-bit serial data in the semicustom IC. This makes all functions of the the servo circuit constant. It works at the "L" level.
16	$\overline{CS}$	I	SELECT terminal for the data from the microprocessor (IC10). At the "L" level, the DCK operation is accepted and the data is taken into the internal latch at the leading edge. (¯⌊_↑¯)
*13	TPO	I	TES polarity setting terminal. The counter clock to determine the kick amount is generated at "_⌈¯↓_" of TES input signal in FWD KICK at the "H" level and at "_↑¯⌊_" at the "L" level.
11	KICF	O	Output terminal of pulse to feed PU outward. This is used to kick the tracking coil and PU motor. ' It works at the "H" level and stops at the "L" level.

Table 4-2-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

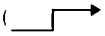
Pin No.	Name	I/O	Function
12	$\overline{KICB}$	O	Output terminal of pulse of feed PU inward. This is used to kick the tracking coil and PU motor. It works at the "L" level and stops at the "H" level.
17	EOK	O	Clock counter to indicate the end of kick or every 32 tracks. This is the signal () to inform the microprocessor that the tracks specified by the microprocessor (IC10) have been kicked.
3	PUFF	O	This rapidly feeds PU outward. It works at the "H" level and stops at the "L" level by the instructions from the microprocessor (IC10).
4	$\overline{PUFB}$	O	This rapidly feeds PU inwafd. It works at the "L" level and stops at the "H" level by the instructions from the microprocessor (IC10) .
5	FEED	O	PU feed (play) output terminal. This is used to turn on and off the feed servo by the instructions from the microprocessor (IC10). ON at the "H" level.
10	TRON	O	This is the signal to turn on and off the TE servo system operation. It works by the instructions from the microprocessor (IC10). It automatically starts operation at the feed KICK and terminates by the instructions from the microprocessor (IC10) (KICK STOP).
26	$\overline{RDY}$	O	Normal play wait signal. "H" level only for normal playing and "L" level for the other modes. It is controlled by the instructions from the microprocessor (IC10).
23	NC		Idle terminal
9	$\overline{KGC}$	O	Terminal to control gain in kick operation. This works at the "L" level. It is automatically sent at the kick operation.
25	FGI	I	Input terminal of the pulse signal coming from FG (frequency generator attached to the disc motor). This is used to detect the dropout position, etc.
24	FGO	O	3-dividing output terminal of FGI. This is used to detect the dropout position, etc.
19	DCK	I	Data clock. This is the transmission clock synchronized with the 8-bit data output from the microprocessor (IC10).
21	V_{DD}	I	Power terminal (+5 V).

Table 4-2-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

- **CODE TABLE**

a) KIC mode

CODE					STATE
3	2	1	0	H	
0	0	0	0	0	KIC STOP (KIC STP)
0	0	0	1	1	FWD 1 TRACK KIC (KIC F01)
0	0	1	0	2	3 (KIC F03)
0	0	1	1	3	5 (KIC F05)
0	1	0	0	4	7 (KIC F07)
0	1	0	1	5	15 (KIC F15)
0	1	1	0	6	31 (KIC F31)
0	1	1	1	7	FWD CONTINUE (EOK inverted every 32)
1	0	0	0	8	KIC STOP
1	0	0	1	9	BWD 1 TRACK KIC (KIC B01)
1	0	1	0	A	3 (KIC B03)
1	0	1	1	B	5 (KIC B05)
1	1	0	0	C	7 (KIC B07)
1	1	0	1	D	15 (KIC B15)
1	1	1	0	E	31 (KIC B31)
1	1	1	1	F	BWD CONTINUE (EOK inverted every 32)

Table 4-2-2

c) Format

- MODE
  - KIC mode ....Used to set the kick direction and amount or to perform the search operation.
  - CONTROL mode ....Signal to control laser, tray, servo systems other than the above ones, etc.

- Bit array

7	6	5	4	3	2	I	0
Control mode				**KIC mode**			

b) CONTROL mode

CODE					STATE										FUNCTION	
7	6	5	4	H	MSR	TRYO	TRYC	PUFF	PUFB	FEED	LDC	TRON	RDY	KGC		
0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	This stops or does not work at all.	RSTM
0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	This closes the tray only.	CLTRYM
0	0	1	0	2	0	1	0	0	1	0	0	0	0	0	This opens the tray only.	OPTRYM
0	0	1	1	3	0	0	1	0	0	0	0	0	0	0	This closes the tray and returns the PU to SLT.	CLPUBM
0	1	0	0	4	0	1	0	0	0	0	0	0	0	0	This opens the tray and returns the PU to SLT.	OPPUBM
0	1	0	1	5	0	0	0	1	1	0	0	0	0	0	This feeds the PU at high speed.	PUFWDM
0	1	1	0	6	0	0	0	0	0	0	0	0	0	0	This returns the PU at high speed.	PUBWDM
0	1	1	1	7	0	0	0	0	1	0	1	0	0	0	This detects presence or absence of disc.	DISCCM
1	0	0	0	8	1	0	0	0	1	0	1	0	0	0	This closes the focus servo.	FORCSM
1	0	0	1	9	1	0	0	0	1	0	1	1	0	1	This closes the tracking servo.	TRACKM
1	0	1	0	A	1	0	0	0	1	1	1	1	1	1	Normal play.	PLAYM
1	0	1	1	B	1	0	0	1	1	0	1	0	0	0	This feeds the PU only. (long search, high-speed feed)	PUFFM
1	1	0	0	C	1	0	0	0	0	0	1	0	0	0	This returns the PU only. (long search, high-speed feed)	PUFBM
1	1	0	1	D	1	0	0	*	*	*	1	*	0	*	KIC operation (short search)	KICM
1	1	1	0	E	1	0	0	0	1	0	0	0	0		This code is not used.	
1	1	1	1	F	1	0	0	0	1	0	0	0	0		This code is not used.	

Notes: **Description of terms used in the above table.**

1) The symbol "STATE" describes the actual signal level.
2) In the items marked with an asterisk "*", is changed to "0" or "1" according to the contents of KICK operation.

Table 4-2-3

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

d) Timing of input data

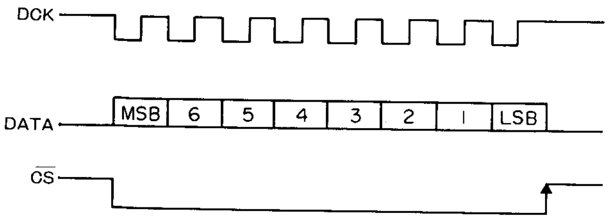


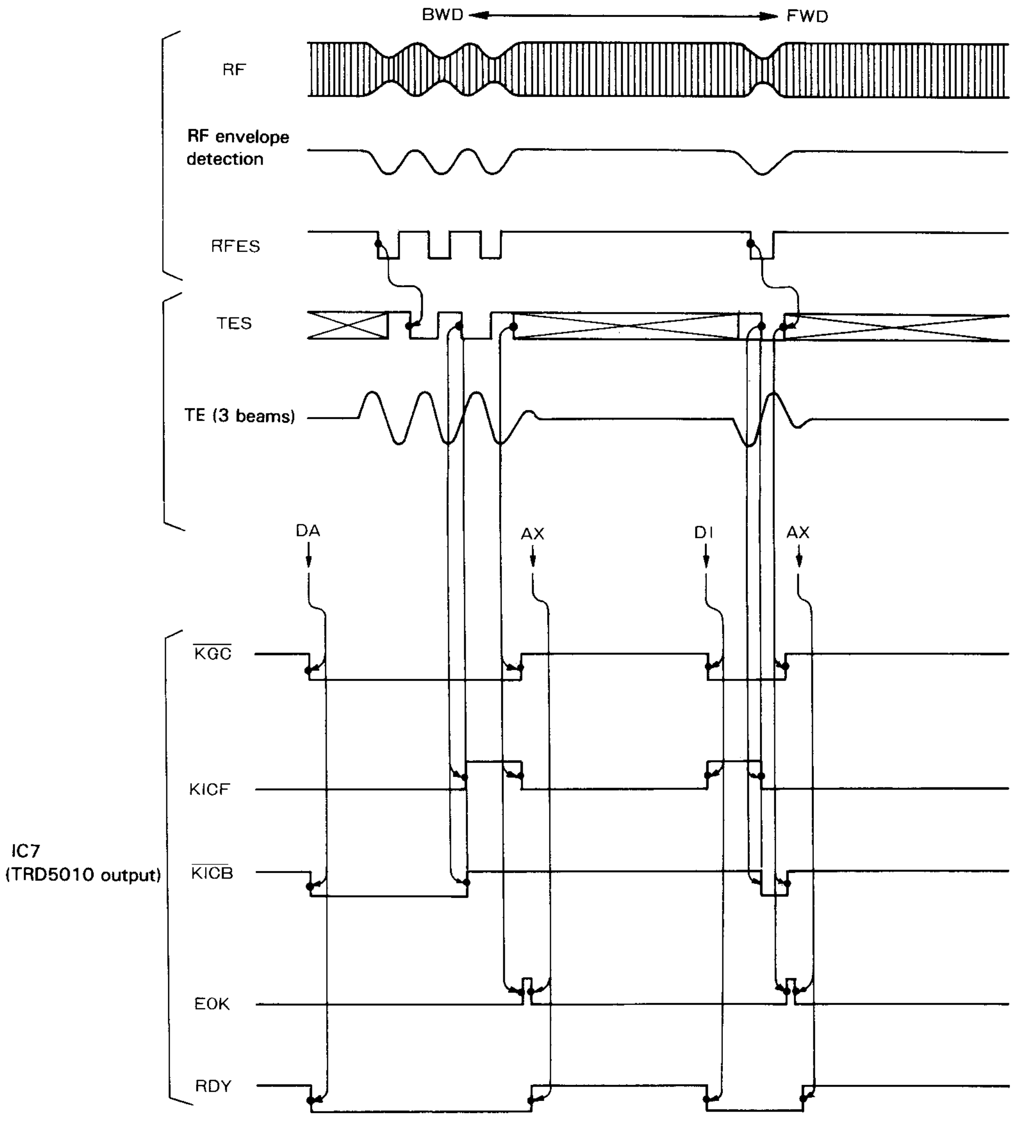
Fig. 4-2-2

e) KICF and $\overline{\text{KICB}}$ work when the KIC amount is less than 31 (active low) in the KIC mode and do not work if it is 31 or more. KICF is usually at the "L" level and becomes "H" level when it works. KICB is usually at the "H" level and becomes "L" level when it works.

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

- **Examples of Operation of RFES and TES Waveforms: 3 Track BWD → 1 Track FWD**

1. **High frequency waveform (RF) and shaped waveform (RFES) and tracking error waveform (TE) and shaped waveform (TES)**


BWD
FWD
RF
RF envelope detection
RFES
TES
TE (3 beams)
DA
AX
DI
AX
IC7
(TRD5010 output)
KGC
KICF
KICB
EOK
RDY

* All the signals other than those shown above do not change.

Fig. 4-2-3

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

2. Timing of control output generated from the semicustom IC in kicks of more than 32 tracks and less than 31 tracks

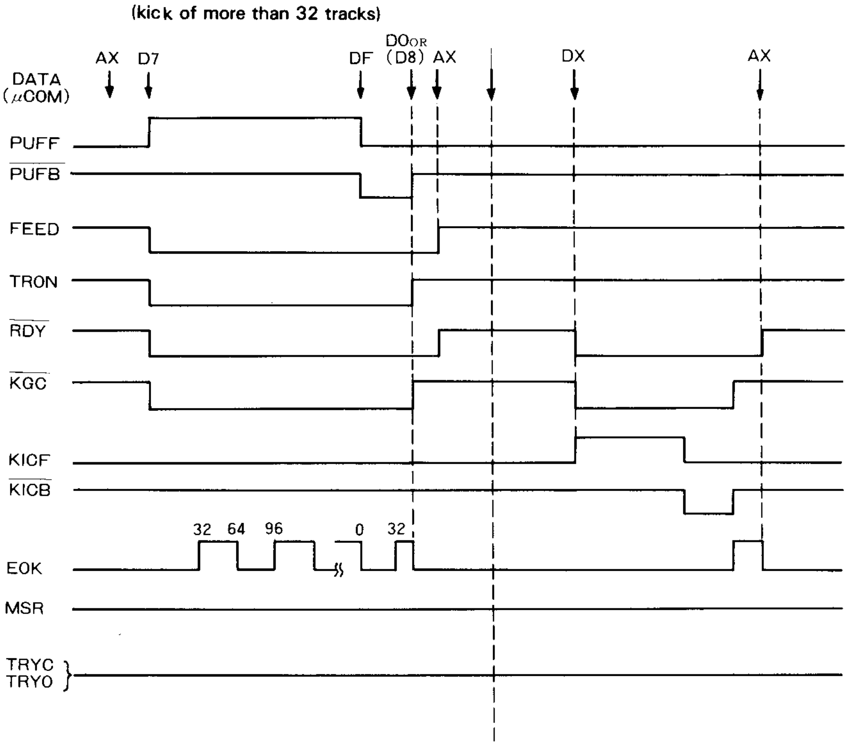

(kick of more than 32 tracks)
DATA (μCOM)
AX
D7
DF
D0 or (D8)
AX
DX
AX
PUFF
PUFB
FEED
TRON
RDY
KGC
KICF
KICB
32
64
96
0
32
EOK
MSR
TRYC
TRYO

Fig. 4-2-4

Notes:
- X in DATA means don't care.
- In the kick operation of more than 32 tracks, the data after the end of PUFF and PUFB operations should be set to the STOP state (D0, D8).
- In the kick operation of more than 32 tracks, start of KICF and $\overline{\text{KICB}}$ operations is automatically switched by the counter in the semicustom IC by informing the TES pulse according to the set amount of data.

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-3 Microprocessor: IC10 (μPD7519G-167-36)

Pin connection

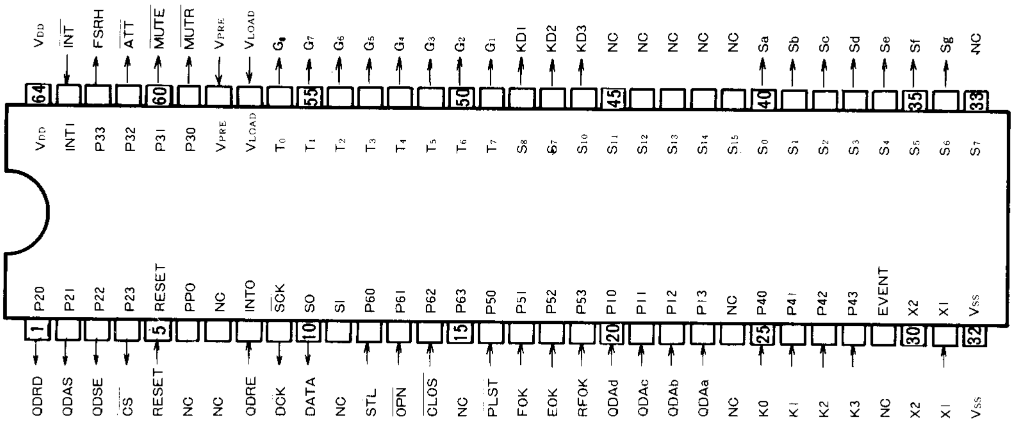


Fig. 4-3-1
(Top view)

Block diagram

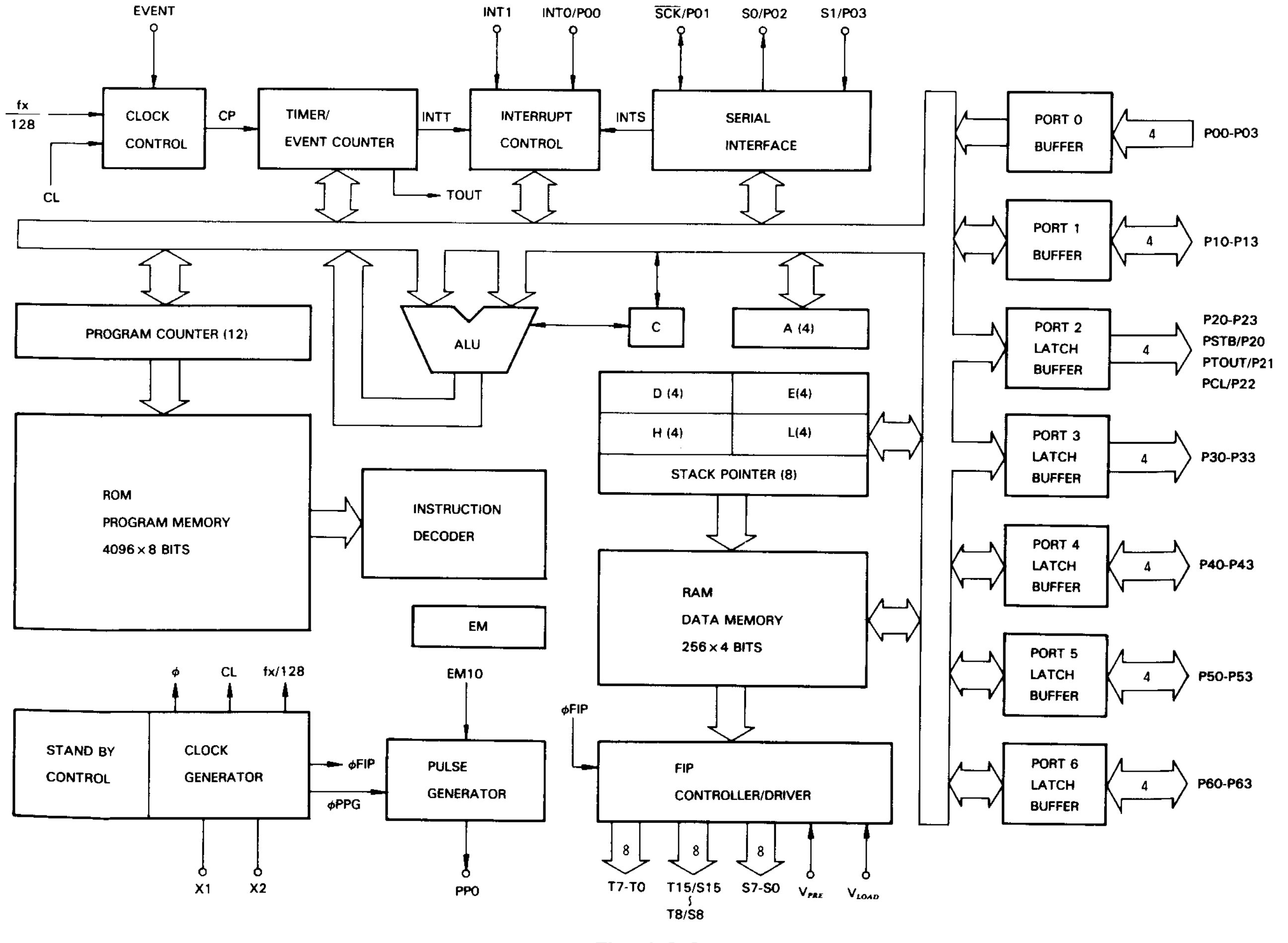

EVENT
INT1
INT0/P00
SCK/P01
S0/P02
S1/P03
fx/128
CL
CLOCK CONTROL
CP
TIMER/ EVENT COUNTER
INTT
INTERRUPT CONTROL
INTS
SERIAL INTERFACE
TOUT
PORT 0 BUFFER
P00-P03
PORT 1 BUFFER
P10-P13
PORT 2 LATCH BUFFER
P20-P23
PSTB/P20
PTOUT/P21
PCL/P22
PORT 3 LATCH BUFFER
P30-P33
PORT 4 LATCH BUFFER
P40-P43
PORT 5 LATCH BUFFER
P50-P53
PORT 6 LATCH BUFFER
P60-P63
4
PROGRAM COUNTER (12)
ALU
C
A (4)
D (4)
E(4)
H (4)
L(4)
STACK POINTER (8)
ROM
PROGRAM MEMORY
4096×8 BITS
INSTRUCTION DECODER
EM
RAM
DATA MEMORY
256×4 BITS
φ
CL
fx/128
EM10
φFIP
STAND BY CONTROL
CLOCK GENERATOR
φPPG
PULSE GENERATOR
FIP CONTROLLER/DRIVER
8
X1
X2
PPO
T7-T0
T15/S15 ~ T8/S8
S7-S0
VPRE
VLOAD

Fig. 4-3-2

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description

Pin. No.	Port		Signal name	I/O	Initial value	Function
1	Port 2	P20	QDRD	O	0	This is the signal to read the Q-data in 4-bit units.
2		P21	QDAS	O	0	This is the signal to switch the CRC check data and Q-data.
3		P22	QDSE	O	0	This is the OUTPUT CONTROL signal of Q-data signal.
4		P23	$\overline{CS}$	O	1	This is the DATA SELECT signal to be sent to TRD5010.
5			RESET	I		This is the initialize start signal.
6			NC			
7			NC			
8	Port 0	INTO	QDRE	I		This is the signal to permit Q-data reading.
9		$\overline{SCK}$	$\overline{DCK}$	O	1	This is the signal to send the data to TRD5010.
10		SO	DATA	O	*	This is the DATA signal to be sent to TRD5010.
11		SI	NC			
12	Port 6	P60	$\overline{SLT}$	I		This is the signal to detect the PU position.
13		P61	$\overline{OPN}$	I		This is the signal to open the tray.
14		P62	$\overline{CLOS}$	I		This is the signal to close the tray.
15		P63	NC			
16	Port 5	P50	$\overline{PLST}$	I		Test mode select signal
17		P51	FOK	I		Focus OK signal
18		P52	EOK	I		End-of-kick signal from TRD5010
19		P53	RFOK	I		RF OK signal
20	Port 1	P10	QDAd	I		Q-data input signal
21		P11	QDAc	I		Q-data input signal
22		P12	QDAb	I		Q-data input signal
23		P13	QDAa	I		Q-data input signal
24			NC			
25	Port 4	P40	K0	I		Key matrix signal
26		P41	K1	I		Key matrix signal
27		P42	K2	I		Key matrix signal
28		P43	K3	I		Key matrix signal
29			NC			
30		X2	X2	O		Clock signal
31		X1	X1	I		Clock signal
32		V_{ss}	V_{ss}	Power supply		Power supply (0 V)
33	Segment		NC			
34		S_6	Sg	O	0	FL segment signal
35		S_5	Sf	O	0	FL segment signal
36		S_4	Se	O	0	FL segment signal
37		S_3	Sd	O	0	FL segment signal
38		S_2	Sc	O	0	FL segment signal
39		S_1	Sb	O	0	FL segment signal
40		S_0	Sa	O	0	FL segment signal
41			NC			
42			NC			
43			NC			
44			NC			
45			NC			
46		S_{10}	KD_3	O	1	Key matrix signal
47		S_9	KD_2	O	1	Key matrix signal
48		S_8	KD_1	O	1	Key matrix signal

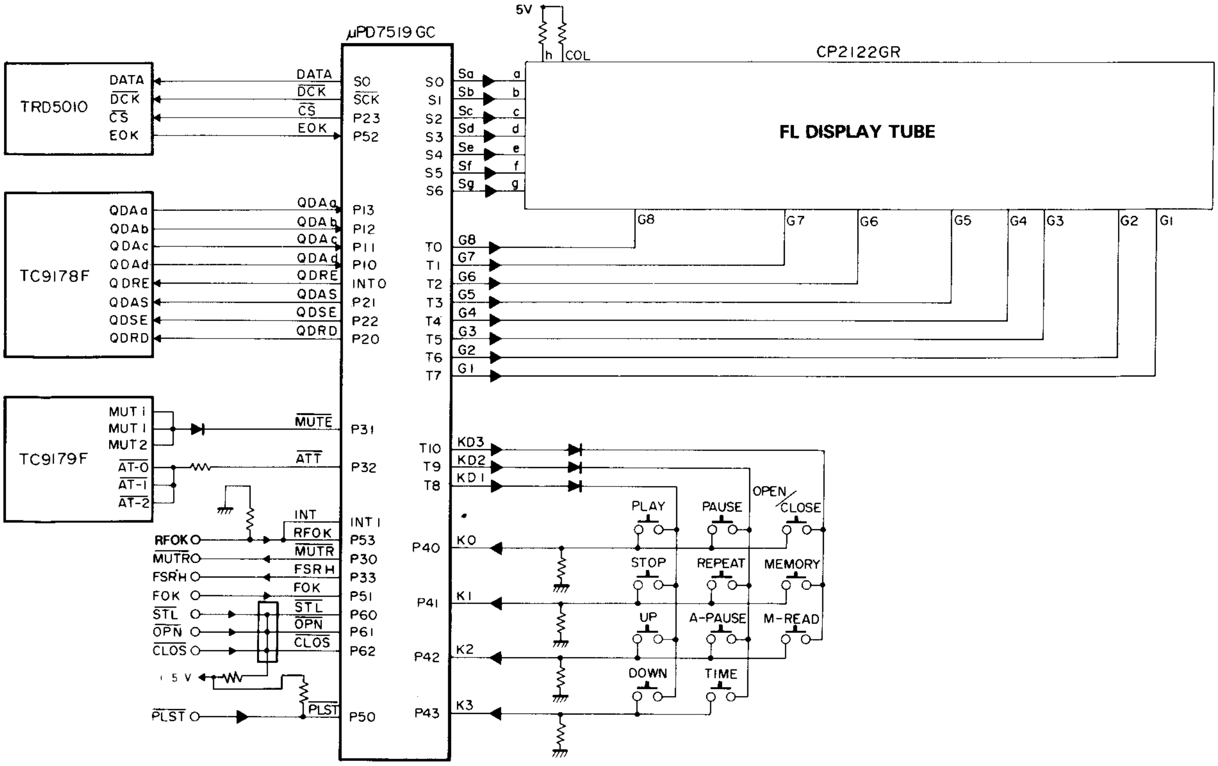
Table 4-3-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin. No.	Port		Signal name	I/O	Initial value	Function
49	Timing	T_7	G1	O	*	FL grid signal
50		T_6	G2	O	*	FL grid signal
51		T_5	G3	O	*	FL grid signal
52		T_4	G4	O	*	FL grid signal
53		T_3	G5	O	*	FL grid signal
54		T_2	G6	O	*	FL grid signal
55		T_1	G7	O	*	FL grid signal
56		T_0	G8	O	*	FL grid signal
57		V_{LOAD}	V_{LOAD}	I		Power supply (−30 V) for FL driver
58		V_{PRE}	V_{PRE}	I		Power supply (0 V) for FL driver
59	Port 3	P30	$\overline{\text{MUTR}}$	O	L	Relay mute signal
60		P31	$\overline{\text{MUTE}}$	O	L	Digital mute signal
61		P32	$\overline{\text{ATT}}$	O	L	ATT signal
62		P33	FSRH	O	L	Focus search signal
63		INT1	$\overline{\text{INT}}$	I		STOP state select signal
64		V_{DD}	V_{DD}	Power supply		Power supply (+5 V)

Table 4-3-1

Circumference circuit of microcomputer



5V
μPD7519 GC
h
COL
CP2122GR
FL DISPLAY TUBE
TRD5010
DATA
DCK
CS
EOK
SO
SCK
P23
P52
SO
SI
S2
S3
S4
S5
S6
Sa
Sb
Sc
Sd
Se
Sf
Sg
a
b
c
d
e
f
g
TC9178F
QDAa
QDAb
QDAc
QDAd
QDRE
QDAS
QDSE
QDRD
P13
P12
P11
P10
INT0
P21
P22
P20
T0
T1
T2
T3
T4
T5
T6
T7
G8
G7
G6
G5
G4
G3
G2
G1
TC9179F
MUT i
MUT 1
MUT2
AT-0
AT-1
AT-2
MUTE
ATT
P31
P32
INT
RFOK
MUTR
FSRH
FOK
STL
OPN
CLOS
PLST
INT 1
P53
P30
P33
P51
P60
P61
P62
P50
RFOK
MUTR
FSRH
FOK
STL
OPN
CLOS
+5 V
PLST
T10
T9
T8
KD3
KD2
KD1
P40
P41
P42
P43
K0
K1
K2
K3
PLAY
PAUSE
OPEN/CLOSE
STOP
REPEAT
MEMORY
UP
A-PAUSE
M-READ
DOWN
TIME

Fig. 4-3-3

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-4 PLL IC: IC1 (TD6315AP)

IC1 (TD6315AP), the PLL IC developed for CD system DAD player, consists of a digital phase comparator, a charge pump circuit, an active LPF and a data separation circuit.
The digital phase comparator detects the phase error between the clock pulse obtained from 4-division of the VCO output and the reference of the HF signal (EFMI) emitted from the data slicer. Then, from the charge pump circuit, up and down signals UO and DO are output as phase error data.

Pin connection diagram

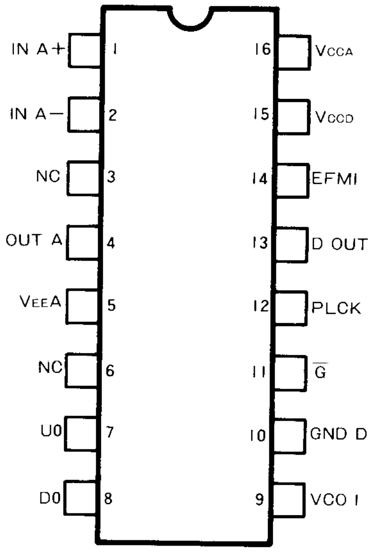

IN A+ 1
IN A− 2
NC 3
OUT A 4
VEEA 5
NC 6
UO 7
DO 8
16 VCCA
15 VCCD
14 EFMI
13 D OUT
12 PLCK
11 $\overline{G}$
10 GND D
9 VCO I

Fig. 4-4-1
(Top view)

Block diagram

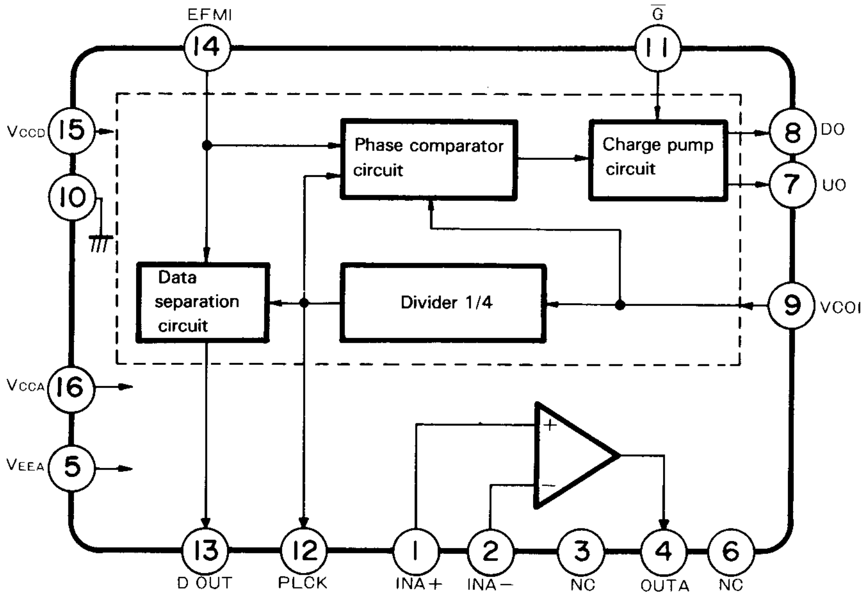

EFMI
14
$\overline{G}$
11
VCCD 15
10
Phase comparator circuit
Charge pump circuit
8 DO
7 UO
Data separation circuit
Divider 1/4
9 VCOI
VCCA 16
VEEA 5
+
−
13 D OUT
12 PLCK
1 INA+
2 INA−
3 NC
4 OUTA
6 NC

Fig. 4-4-2 TD6315AP Block diagram

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description

Pin No.	Symbol	Description	Remarks
1	INA+	Positive input of built-in OP amp. Forms the guard ring of INA− together with pin 3 (NC) fixed to approx. 1/2 V_{CCD} voltage.	
2	INA−	Negative input of built-in OP amp. The signal subject to resistance addition by charge pump circuit outputs UO and DO and TC9178AF pin TMO is input.	
3	NC	Not used. This pin connected to pin INA+for giving isolation between pins INA− and OUTA.	
4	OUTA	Output of built-in OP amp. Connected to pin INA− through capacitor C and resistor R, forms a lag lead type filter to control VCO.	
5	V_{EEA}	Negative voltage supply to analog circuit.	
6	NC	Not used. Connected to pin INA+for giving isolation between pin V_{EEA} and each of output pins UO and DO.	
7	UO	Charge pump up signal output pin. When signal PLCK obtained from 4-division of VCO frequency is phase delayed in rising edge against signal EFMI input, its "L" output duration is prolonged to make VCO frequency higher. In phase lock, "L" level = 1/2 PLCK.	High impedance state except during "L" direction.
8	DO	Charge pump down signal output pin. When signal PLCK obtained from 4-division of VCO frequency is phase advanced in rising edge against signal EFMI input, its "H" output duration is prolonged to make VCO frequency lower. In phase save, "H" level = 1/2 PLCK.	High impedance state except during "H" period
9	VCOI	Input pin of VCO output signal. The signal subject to AC coupling by a capacitor is input.	
10	GND	GND pin for digital circuit	
11	G	Input by which charge pump outputs UO and DO are made into high impedance. When made "L", high impedance mode is entered to hold the VCO frequency.	TTL level
12	PLCK	Output of data separation clock pulse generated from EFMI input signal in PLL circuit. This output, obtained from 4-division of VCO frequency (17.3 MHz), is input to PLCK of C-MOS processor TC9178F. The clock pulse is 4.32 MHz with duty ratio of 50.	C-MOS leve

Table 4-4-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin No.	Symbol	Description	Remarks
13	DOUT	Signal EFMI output. This output, synchronized with the rising edge of signal PLCK, is input to pin EFMI of C-MOS processor TC9178F.	C-MOS level
14	EFMI	Input for EFMI signal obtained by passing the RF signal regenerated from disc through data slicer.	TTL level
15	V_{CCD}	Voltage supply to digital circuit.	
16	V_{CCA}	Positive voltage supply pin to analog circuit.	

Table 4-4-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-5 E.F.M decoder: IC2 (TC9178AF)

Pin connection

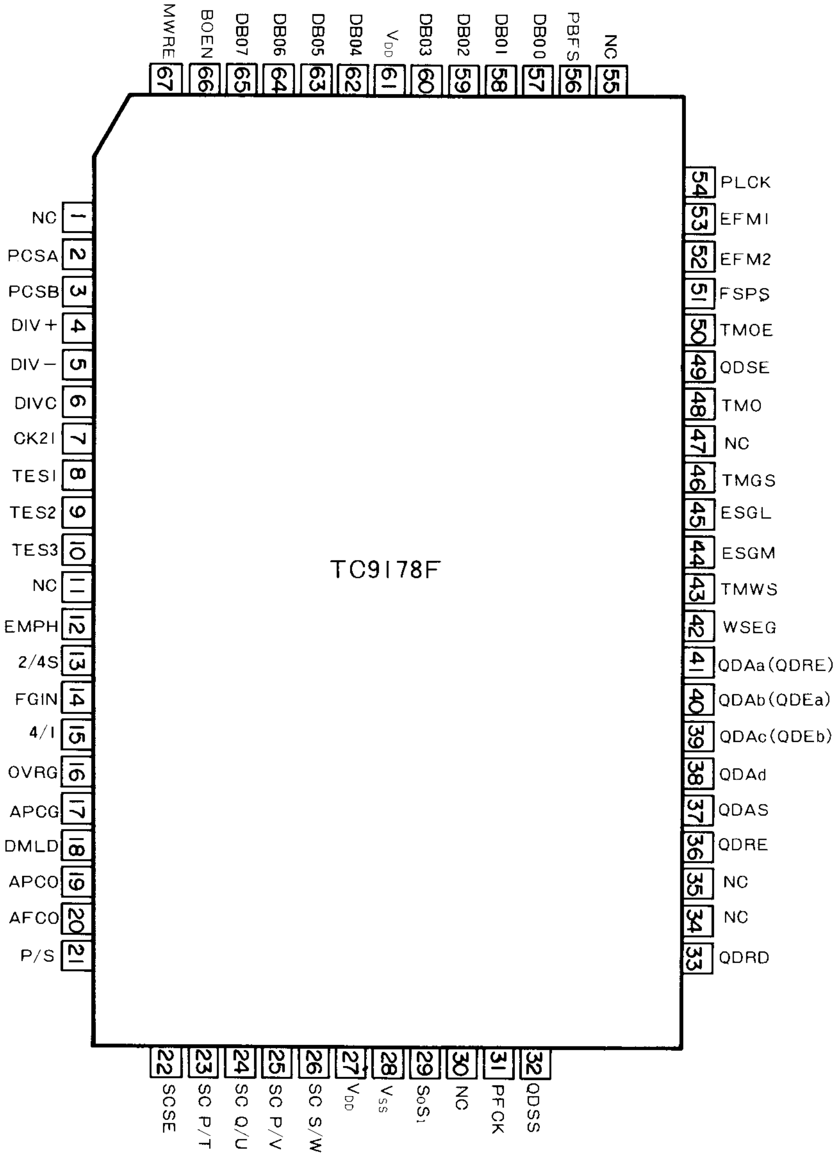

TC9178F
1 NC
2 PCSA
3 PCSB
4 DIV+
5 DIV−
6 DIVC
7 CK21
8 TES1
9 TES2
10 TES3
11 NC
12 EMPH
13 2/4S
14 FGIN
15 4/1
16 OVRG
17 APCG
18 DMLD
19 APCO
20 AFCO
21 P/S
22 SCSE
23 SC P/T
24 SC Q/U
25 SC P/V
26 SC S/W
27 VDD
28 VSS
29 SoS1
30 NC
31 PFCK
32 QDSS
33 QDRD
34 NC
35 NC
36 QDRE
37 QDAS
38 QDAd
39 QDAc (QDEb)
40 QDAb (QDEa)
41 QDAa (QDRE)
42 WSEG
43 TMWS
44 ESGM
45 ESGL
46 TMGS
47 NC
48 TMO
49 QDSE
50 TMOE
51 FSPS
52 EFM2
53 EFM1
54 PLCK
55 NC
56 PBFS
57 DB00
58 DB01
59 DB02
60 DB03
61 VDD
62 DB04
63 DB05
64 DB06
65 DB07
66 BOEN
67 MWRE

Fig. 4-5-1
(Top view)

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

TC9178AF Block diagram

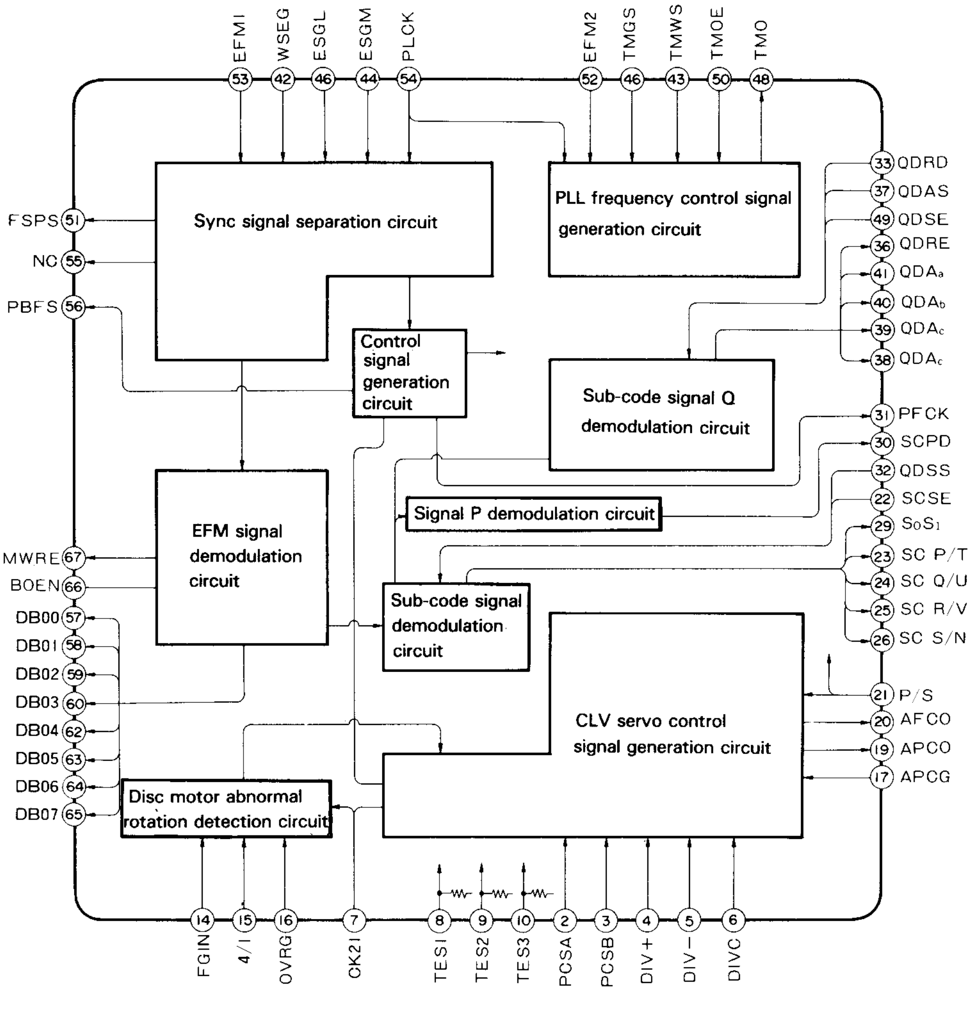
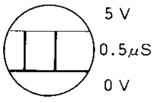
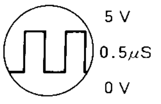

EFMI 53
WSEG 42
ESGL 46
ESGM 44
PLCK 54
EFM2 52
TMGS 46
TMWS 43
TMOE 50
TMO 48
Sync signal separation circuit
PLL frequency control signal generation circuit
Control signal generation circuit
Sub-code signal Q demodulation circuit
EFM signal demodulation circuit
Signal P demodulation circuit
Sub-code signal demodulation circuit
CLV servo control signal generation circuit
Disc motor abnormal rotation detection circuit
FSPS 51
NC 55
PBFS 56
MWRE 67
BOEN 66
DB00 57
DB01 58
DB02 59
DB03 60
DB04 62
DB05 63
DB06 64
DB07 65
33 QDRD
37 QDAS
49 QDSE
36 QDRE
41 QDAa
40 QDAb
39 QDAc
38 QDAc
31 PFCK
30 SCPD
32 QDSS
22 SCSE
29 SoS1
23 SC P/T
24 SC Q/U
25 SC R/V
26 SC S/N
21 P/S
20 AFCO
19 APCO
17 APCG
14 FGIN
15 4/1
16 OVRG
7 CK21
8 TES1
9 TES2
10 TES3
2 PCSA
3 PCSB
4 DIV+
5 DIV−
6 DIVC

Fig. 4-5-2

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>1</td><td>NC</td><td>—</td><td>—</td><td>Not connected</td><td></td></tr>
<tr><td>2</td><td>PCSA</td><td>I</td><td></td><td>These inputs determines the phase comparison frequency.
Phase comparison frequency = 7.35 kHz (frame sync signal)/N
<table>
<tr><th>PCSA</th><th>PCSB</th><th>N</th><th>fc (Hz)</th></tr>
<tr><td>L</td><td>L</td><td>6</td><td>1225</td></tr>
<tr><td>H</td><td>L</td><td>8</td><td>918.75</td></tr>
<tr><td>L</td><td>H</td><td>17</td><td>612.5</td></tr>
<tr><td>H</td><td>H</td><td>16</td><td>459.375</td></tr>
</table></td><td></td></tr>
<tr><td>4</td><td>DIV+</td><td>I</td><td>

(Appears only at low disc rotation.)</td><td rowspan="3">Input for setting reference frequency division coefficient in APC signal generation circuit for CLV servo control.
Input as buffer memory status signal from TC9179F (IC4).
In addition, the varying amount is selectable by DIVC.
<table>
<tr><th>DIV+</th><th>DIV−</th><th>DIVC</th><th>Reference frequency division coefficient</th><th>Disc motor speed</th></tr>
<tr><td>L</td><td>L</td><td>*</td><td>1/288</td><td></td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>1/287.5</td><td>Higher</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>1/287</td><td>Higher</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>1/288.5</td><td>Lower</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>1/289</td><td>Lower</td></tr>
<tr><td>H</td><td>H</td><td>*</td><td>1/288</td><td></td></tr>
</table>
* Don't care</td><td rowspan="3">Connected to each of TC9179F DIV+ (pin 65) and DIV− (pin 64)</td></tr>
<tr><td>5</td><td>DIV−</td><td>I</td><td>

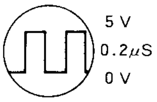
(Appears only at high disc rotation.)</td></tr>
<tr><td>6</td><td>DIVC</td><td>I</td><td></td></tr>
<tr><td>7</td><td>CK21</td><td>I</td><td>
</td><td>2.1168 MHz input. This signal, the clock pulse obtained from 4-division of X'tal OSC frequency 8.4672 MHz, is input from TC9179F (IC4). Its duty ratio is 50.</td><td>Connected to CK2M (pin 56) of TC9179F (IC4)</td></tr>
<tr><td>8～10</td><td>TES-1～TES-3</td><td>I</td><td></td><td>Test inputs, which operates normally at "H" or open state.</td><td>Pullup resistor incorporated</td></tr>
<tr><td>11</td><td>NC</td><td>—</td><td></td><td>Not connected.</td><td></td></tr>
<tr><td>12</td><td>EMPH</td><td>O</td><td></td><td>Output for emphasis presence/absence judgement represented by control bit of sub-code signal Q.
"H" = de-emphasis ON</td><td></td></tr>
</table>

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

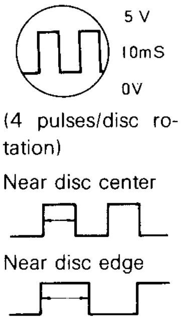
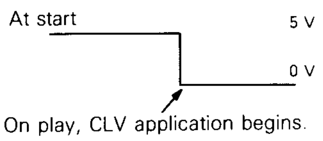
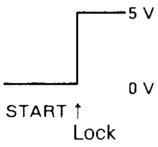
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>13</td><td>2/4S</td><td>O</td><td>—</td><td>Output for CH 2/CH 4 selection judgement represented by control bit of sub-code signal Q.
"L" = CH 2, "H" = CH 4</td><td>Not used</td></tr>
<tr><td>14</td><td>FG IN</td><td>I</td><td> </td><td>Input for FG pulse from disc motor.
1 or 4 pulse per each rotation of disc motor is fed to control speed of the motor within the range of 170 to 400 rpm.
<table>
<tr><th>Disc motor speed (rpm)</th><th>AFCO</th><th>APCO</th></tr>
<tr><td>-175</td><td>Fixed to "H"</td><td>Fixed to 50% duty cycle output</td></tr>
<tr><td>175-740</td><td>Normal operation</td><td>Normal operation</td></tr>
<tr><td>740-</td><td>Fixed to "L"</td><td>Fixed to 50% duty cycle output</td></tr>
</table></td><td>Not used</td></tr>
<tr><td>15</td><td>4/1</td><td>I</td><td></td><td>FG IN pulse setting. Either of 1 or 4 pulse per each rotation can be set.
<table>
<tr><th>4/1</th><th>FG pulse per each disc motor rotation</th></tr>
<tr><td>"H" level</td><td>1</td></tr>
<tr><td>"L" level</td><td>4</td></tr>
</table></td><td>GND</td></tr>
<tr><td>16</td><td>OVRG</td><td>I</td><td> </td><td>Pin to select whether or not disc motor rotation control is performed by FG IN input.
"H" - FG IN input valid
"L" - FG input not valid</td><td>GND</td></tr>
<tr><td>17</td><td>APCG</td><td>I</td><td>"H"</td><td>ON/OFF selection input of APC signal generator for CLV servo control.
"L" (generator OFF): APC output is fixed to phase difference "0" that is duty ratio of 50. At the same time, as the internal phase comparison reference frequency generation section is arranged into phase difference "0" against the controlled frequency, the start point of phase comparison when the generator is changed from OFF to ON is set to phase difference "0".</td><td></td></tr>
<tr><td>18</td><td>DMLD</td><td>O</td><td> </td><td>Disc motor lock detection output of AFC signal generator for CLV servo control.
Detects the frequency of the frame sync signal. When the frequency is within ±5% deviation, it is set. When the frequency is over ±10 deviation, it is reset. This output signal is the flip-flop output signal. When set, this flip-flop output becomes "H". This output, connected to pin APCG, is used for control of APC block.</td><td></td></tr>
</table>

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

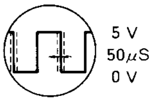
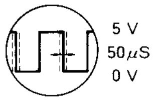
Pin No.	Symbol	I/O	Waveform	Description	Remarks
19	APCO	O		APC signal output for CLV servo control. The output is a PWM (Pulse Width Modulation) wave with resolution = 8 bits, carrier frequency = 8.27 kHz and linear output range = 8 $\pi/9$.	
20	AFCO	O		AFC signal output for CLV servo control. The output is a PWM wave with resolution = 8 bits, carrier frequency = 8.27 kHz and linear output range = ±10%.	
21	P/S	I	"H"	CLV servo control signal ON/OFF input. At play, this pin is set to "H" and, at stop, to "L". This input signal is given the highest priority in the CLV servo control system. When this pin is "L", AFC output is fixed to "L", and APC output gets duty ratio of 50.	Connected to MSR (pin 6) of TRD5010 (IC7)
22	SCSE	I	—	Data selection input for 4 outputs of sub-code signal SCT/T - S/W "L" level: Data of 4 bits, P, Q, R and S is output. "H" level: Data of 4 bits T, U, V and W is output.	
23-26	SC P/T SC Q/U SC R/V SC S/W	O	—	8-bit data output of sub-code signal P, Q, R, S, T, U, V, W. This signal is the data of each frame. Here, 4-bit data is output by signal SCSE as required. Data selection of each frame is performed in synchronization with the rising edge of signal PFCK.	
27	V_{DD}	—	—	Voltage supply pin.	
28	V_{SS}	—	—	GND pin	
29	S_0S_1	O	—	When sub-code signal pattern SO or S1 is detected, this output becomes "H" for that input frame period.	
30	SCPD	O	—	Output to indicate the date contents of sub-code signal P. Data obtained when the data of each frame is checked in units of 5 frames by the sub-code signal P detection section is output.	
31	PFCK	O	—	The frame period output with duty ratio of 50. The sub-code data is switched in synchronization with the falling edge of this output.	

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

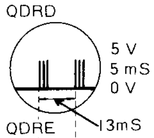
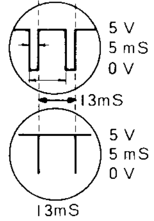
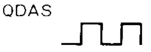
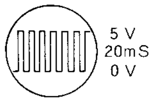
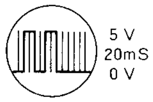
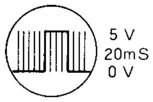
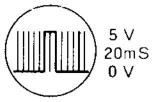
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>32</td><td>QDSS</td><td>I</td><td>"L"</td><td>Input for sub-code sync pattern detection mode selection, demodulating sub-code signal Q.</td><td></td></tr>
<tr><td>33</td><td>QDRD</td><td>I</td><td> </td><td>Input used in reading the sub-code signal Q data inside internal memory in units of 4 bits via outputs QDA-a to QDA-d. When signal QDRD becomes "H", the next 4-bit data is set to pins QDA-a to QDA-d after an arbitrary period from that pulse edge.</td><td></td></tr>
<tr><td>36</td><td>QDRE</td><td>O</td><td> </td><td>Enable signal output reading sub-code signal Q. When error judgement of 80-bit input sub-code signal Q data is completed, those 4-bit data of MSB side are set to pin QDA-a to QAD-d, and output QDRE becomes "H".
When 20 pulses are input to QDRD or when data Q in the next block is written before the data written in internal RAM is read out, output QDRE becomes "L" so that data reading is disabled.</td><td></td></tr>
<tr><td>37</td><td>QDAS</td><td>I</td><td>
With block error</td><td>Data selection input for sub-code signal Q data outputs QAD-a to QAD-d. For easier interface with the microprocessor, this input determines output data at QDA-a to b, QDRE and QDE ports.
<table>
<tr><th>QDAS \ Port</th><th>QDAa</th><th>QDAb</th><th>QDAc</th><th>QDAd</th></tr>
<tr><td>L</td><td>QDRE</td><td>QDEa</td><td>QDEb</td><td>L</td></tr>
<tr><td>H</td><td>QDAa</td><td>QDAb</td><td>QDAc</td><td>QDAd</td></tr>
</table></td><td></td></tr>
<tr><td>34, 35</td><td>NC</td><td>—</td><td>Not connected.</td><td></td><td></td></tr>
<tr><td>38</td><td>QDA-d</td><td rowspan="4">O</td><td> </td><td rowspan="4">The 80-bit sub-code signal Q data, the block error judgement result of the sub-code signal Q data output or signal QDRE, is output according to the "L" or "H" setting of QDAS. For data transfer to the microprocessor, QDAS is made "L" first, then the error judgement result of data Q is transferred and signal QDRD is input with QDAS "L". Thus, data Q is transferred in units of 4 bits as required.
In addition, QDA-a to QDA-d are 3-state outputs, where selection between output mode and high-impedance mode is made by "L" or "H" of QDSE.
<table>
<tr><th>QDEa</th><th>QDEb</th><th>Result of judgement</th><th>Output data processing</th></tr>
<tr><td>H</td><td>H</td><td>No error</td><td>Direct output</td></tr>
<tr><td>L</td><td>H</td><td>1-bit error of CRCC</td><td>Direct output</td></tr>
<tr><td>H</td><td>L</td><td>1-bit error of data Q</td><td>1-bit correction output</td></tr>
<tr><td>L</td><td>L</td><td>Error of 2 bits or more</td><td>Direct output</td></tr>
</table></td><td rowspan="4"></td></tr>
<tr><td>39</td><td>QDA-c</td><td> </td></tr>
<tr><td>40</td><td>QDA-b</td><td> </td></tr>
<tr><td>41</td><td>QDA-a</td><td>
(Example of waveform)</td></tr>
</table>

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>42</td><td>WSEG</td><td>I</td><td>—</td><td>Window selection of gate signal which, when the frame sync pattern of EFM signal is detected, determines whether or not this pattern is given as the sync signal for the internal system.
<table><tr><th>WSEG</th><th>Gate signal window (number of clocks PLCK)</th></tr><tr><td>L</td><td>±3</td></tr><tr><td>H</td><td>±7</td></tr></table></td><td></td></tr>
<tr><td>43</td><td>TMWS</td><td>I</td><td>—</td><td>Selects the number of Tmax = N (PLCK) in detection of T_{max} of EFM signal which is input from pin EFM2.
<table><tr><th>TMWS</th><th>N (PLCK)</th></tr><tr><td>L</td><td>11±1</td></tr><tr><td>H</td><td>11±0.5</td></tr></table></td><td></td></tr>
<tr><td>44</td><td>FSGM</td><td rowspan="2">I</td><td rowspan="2">—</td><td rowspan="2">When no frame sync pattern is detected within the window of the frame sync separation protection gate signal in N continuous frames, system synchronization is made by the next input frame sync pattern without the window.
These two inputs are used in selection of number N.
<table><tr><th>FSGL</th><th>FSGM</th><th>N (frame)</th></tr><tr><td>L</td><td>L</td><td>12</td></tr><tr><td>H</td><td>L</td><td>8</td></tr><tr><td>L</td><td>H</td><td>4</td></tr><tr><td>H</td><td>H</td><td>2</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td>45</td><td>FSGL</td></tr>
<tr><td>46</td><td>TMGS</td><td>I</td><td>—</td><td>To prevent faulty Tmax detection, data is valid only when data Tmax continues N times. This number N is determined by the input.
<table><tr><th>TMGS</th><th>N</th></tr><tr><td>L</td><td>7</td></tr><tr><td>H</td><td>4</td></tr></table></td><td></td></tr>
<tr><td>47</td><td>NC</td><td>—</td><td>—</td><td>Not connected.</td><td></td></tr>
</table>

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

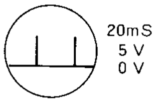
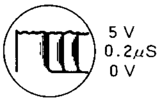
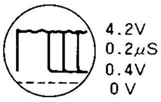
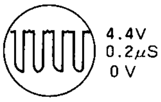
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>48</td><td>TMO</td><td>O</td><td>"DC 2.5 V" ~3.0 V</td><td>The frequency data obtained from T_{max} detection of EFM signal which is input from EFM2 is output in one of 3 states as the result of comparison between signal PLCK and T_{max}. This output can be used as the frequency status for the PLL circuit.
When P/S signal is "L" (stop mode), output TMO is compulsorily fixed to "H".
<table>
<tr><th>EFM signal frequency status</th><th>TMO</th></tr>
<tr><td>$f_{Tmax} > f_{PLCK}$</td><td>L</td></tr>
<tr><td>$f_{Tmax} \fallingdotseq f_{PLCK}$</td><td>High impedance</td></tr>
<tr><td>$f_{Tmax} > f_{PLCK}$</td><td>H</td></tr>
</table></td><td></td></tr>
<tr><td>49</td><td>QDSE</td><td>I</td><td>"H"</td><td>Input of "H" compulsorily makes outputs QDA-a to QDA-d into high impedance state. This input enables effective use of microprocessor input ports.</td><td></td></tr>
<tr><td>50</td><td>TMOR</td><td>I</td><td rowspan="2">This appears when no synchronization is obtained over some frames.

N= 2</td><td>Input of "L" compulsorily makes output TMO into high impedance state. Normally, it is connected to FSPS or FSLO.</td><td></td></tr>
<tr><td>51</td><td>FSPS</td><td>O</td><td>Output to indicate the system sync state on the frame sync pattern. Becomes "H" when no sync pattern is given within the window of gate signal in N continuous frames on selection by input FSGL or FSGM.</td><td></td></tr>
<tr><td>52</td><td>EFM2</td><td>I</td><td> </td><td>Input of EFM signal regenerated from disc. The signal obtained by slicing the signal from the RF amp by the level comparator is directly input (asynchronous to signal PLCK).</td><td></td></tr>
<tr><td>53</td><td>EFM1</td><td>I</td><td> </td><td>Input for EFM signal regenerated from disc. Differently from input signal EFM2, this signal is synchronized to falling edge of signal PLCK phase-locked in the PLL circuit.</td><td></td></tr>
<tr><td>54</td><td>PLCK</td><td>I</td><td> </td><td>Clock pulse input for frame sync separation. This signal is fed from external PLL circuit based on HF signal reproduced from disc. This Clock pulse signal is locked to 4.32 MHz and have duty ratio of 50.</td><td></td></tr>
</table>

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

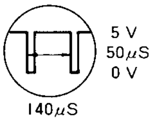
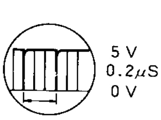
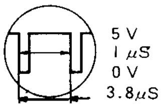
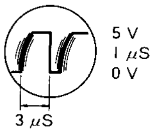
Pin No.	Symbol	I/O	Waveform	Description	Remarks
55	FSLO	O		When each system is in synchronization by the frame sync pattern, and when that input pattern is completely synchronized with the frame sync pattern in internal frame counter (the frame synchronization necessarily has 588 pulses PLCK), "L" is output during the frame period.	Not connected
56	PBFS	O		When "H" is output with a frame sync signal, demodulation data U_0 to U_{31} are transferred to TC9179 (IC6). If "H" which acts as an enable flag, symbol data U_0 to U_{31} transfer will be possible by MWRE.	* Note Connected to PBFS (pin 2) of TC9179F (IC6)
57 ~ 60 62 ~ 65	DBOO- DB07	O		Outputs for demodulation data U_0 to U_{31} in each frame. These are 3-state outputs. When pin BOEN is "L", data is output. DBOO (LSB) to DB07 (MSB)	* Note Connected to I/O 0 - 7 (pins 19-26) of TC9179F (IC6)
66	BOEN	I		Input for enable signal which turns ON the DBOO to BD07 bus driver.	* Note Connected to BOEN (pin 4) of TC9179F (IC6)
67	MWRE	O		Output for the enable signal which makes memory write enable. Becomes "L" at the timing at which data is set to the DBOO to DB07 data transfer register. When pin BOEN is "H" and it becomes "L" when pin MWRE becomes "H". After signal PBFS becomes "H", it emits 32 outputs every 17 clock pulses PLCK.	DBOO

Table 4-5-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-6. Error correction: IC4 (TC9179F)

Pin connection

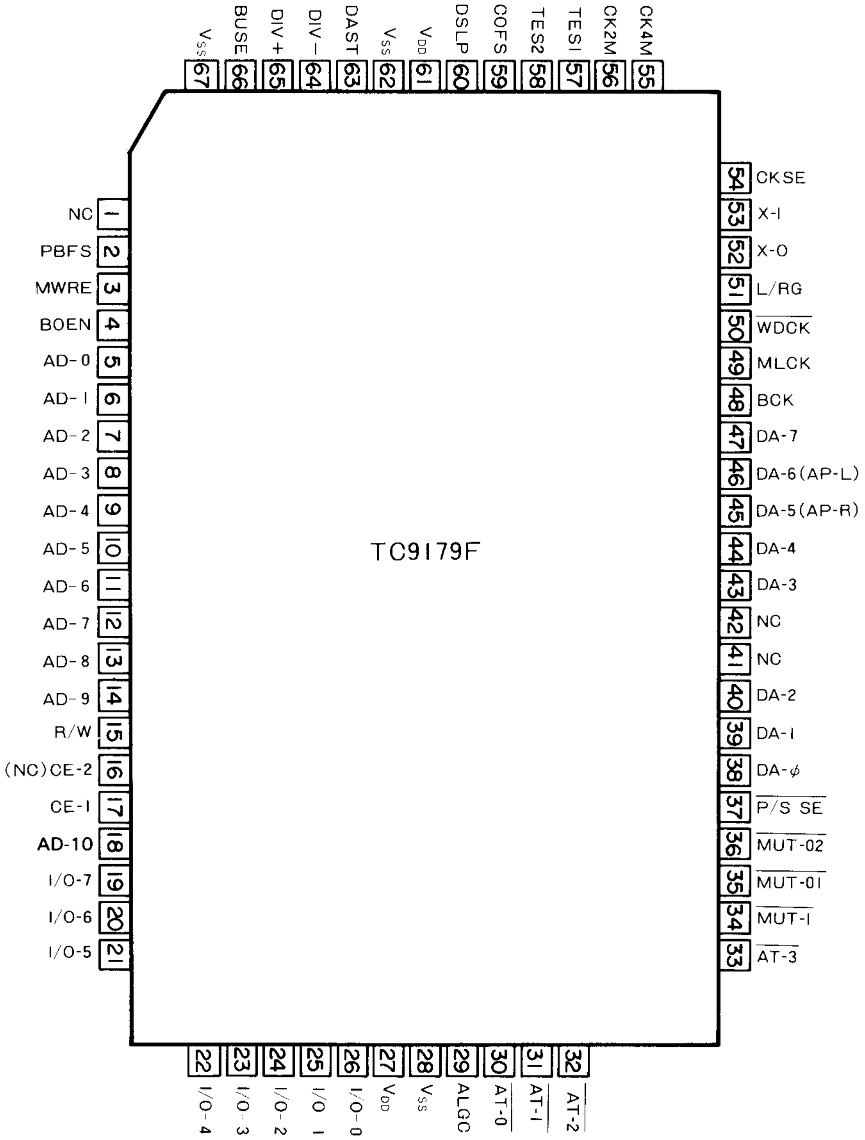
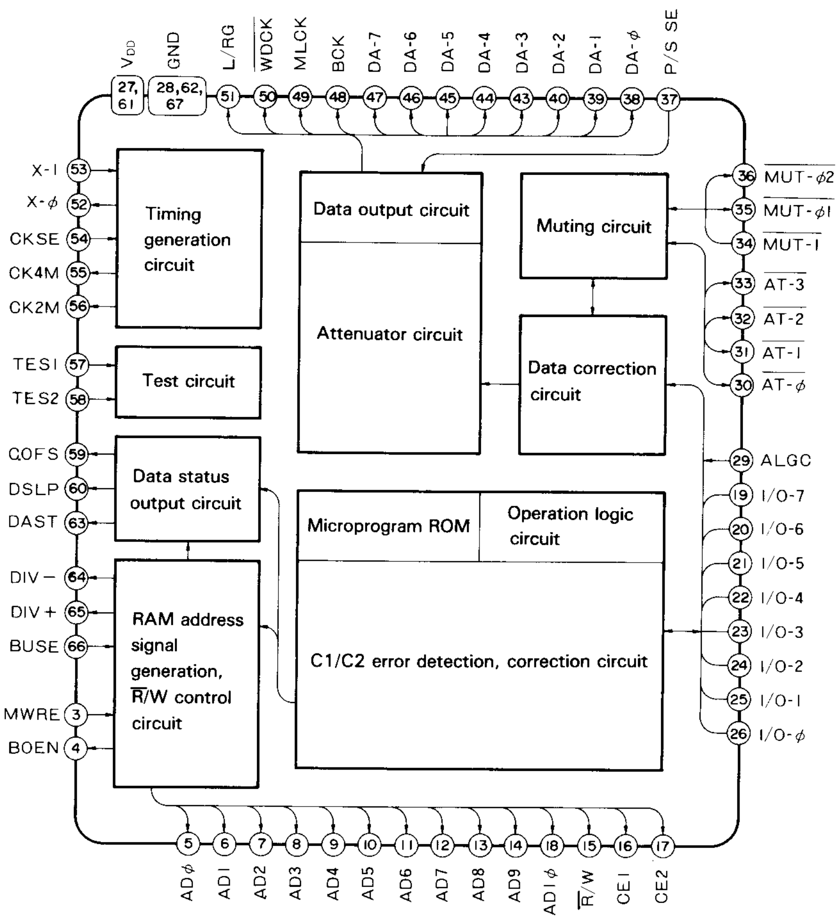

TC9179F
1 NC
2 PBFS
3 MWRE
4 BOEN
5 AD-0
6 AD-1
7 AD-2
8 AD-3
9 AD-4
10 AD-5
11 AD-6
12 AD-7
13 AD-8
14 AD-9
15 R/W
16 (NC)CE-2
17 CE-1
18 AD-10
19 I/O-7
20 I/O-6
21 I/O-5
22 I/O-4
23 I/O-3
24 I/O-2
25 I/O-1
26 I/O-0
27 VDD
28 VSS
29 ALGC
30 AT-0
31 AT-1
32 AT-2
33 AT-3
34 MUT-I
35 MUT-01
36 MUT-02
37 P/S SE
38 DA-φ
39 DA-1
40 DA-2
41 NC
42 NC
43 DA-3
44 DA-4
45 DA-5(AP-R)
46 DA-6(AP-L)
47 DA-7
48 BCK
49 MLCK
50 WDCK
51 L/RG
52 X-O
53 X-I
54 CKSE
55 CK4M
56 CK2M
57 TES1
58 TES2
59 COFS
60 DSLP
61 VDD
62 VSS
63 DAST
64 DIV−
65 DIV+
66 BUSE
67 VSS

Fig. 4-6-1
(Top view)

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Block diagram


V_DD
GND
L/RG
WDCK
MLCK
BCK
DA-7
DA-6
DA-5
DA-4
DA-3
DA-2
DA-1
DA-φ
P/S SE
27, 61
28,62, 67
51
50
49
48
47
46
45
44
43
40
39
38
37
X-1 53
X-φ 52
CKSE 54
CK4M 55
CK2M 56
TES1 57
TES2 58
QOFS 59
DSLP 60
DAST 63
DIV− 64
DIV+ 65
BUSE 66
MWRE 3
BOEN 4
Timing generation circuit
Test circuit
Data status output circuit
RAM address signal generation, R/W control circuit
Data output circuit
Attenuator circuit
Muting circuit
Data correction circuit
Microprogram ROM
Operation logic circuit
C1/C2 error detection, correction circuit
36 MUT-φ2
35 MUT-φ1
34 MUT-1
33 AT-3
32 AT-2
31 AT-1
30 AT-φ
29 ALGC
19 I/O-7
20 I/O-6
21 I/O-5
22 I/O-4
23 I/O-3
24 I/O-2
25 I/O-1
26 I/O-φ
5 ADφ
6 AD1
7 AD2
8 AD3
9 AD4
10 AD5
11 AD6
12 AD7
13 AD8
14 AD9
18 AD1φ
15 R/W
16 CE1
17 CE2

φ=0

Fig. 4-6-2 TC9179F Block diagram

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Pin description

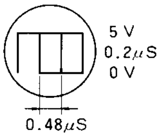
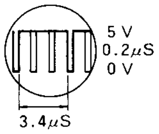
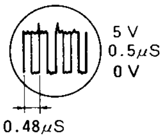
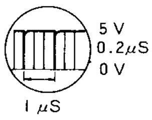
Pin No.	Symbol	I/O	Waveform	Description	Remarks
27, 61	V_{DD}	—	—	Voltage supply pin	
28, 62, 67	V_{SS}	—	—	GND pin	
2	PBFS	I	—	Frame sync input. The symbol data period signal of each frame sent from TC9178AF (IC2) is input.	Connected to PBFS (pin 56) of TC9178AF (IC2)
3	MWRE	I	—	Memory write request input which accepts MWRE signal from TC9178AF (IC2)	Connected to MWRE (pin 67) of TC9178AF (IC2)
4	BOEN	O	—	Output enable. When signal MWRE from TC9178AF (IC2) can be accepted, the control signal to release symbol data output DB00 to DB07 from Hi-impedance state is output.	Connected to BUSE (pin 66) of TC9178AF (IC2)
5~14, 18	AD0~AD9, AD10	O		External RAM address data output. Connected to address data input of external RAM.	
15	$\overline{R}$/W	O		Read/write signal output to external RAM. Connected to $\overline{R}$/W input of external RAM. "L" = Read, "H" = Write	
16	CE2	O		Chip enable 2 signal is output when external RAM is read or written. Connected to CE2 input of external RAM.	Not connected
17	CE1	O		Chip enable 1 signal is output when external RAM is read or written. Connected to CE1 input of external RAM.	
19~26	I/O-7~ I/O-0	I/O		Data bus line connected to I/O-0 to 7 of external RAM and DB04 -DB07 of TC9178AF (IC2).	

Table 4-6-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th>Description</th><th>Remarks</th></tr>
<tr><td>29</td><td>ALGC</td><td>I</td><td>—</td><td>Process selection input of C2 correction section. Selects the process algorithm for the frame in which detection of error symbol is not possible in C2 correction section. It is "L" in normal operation.</td><td>Connect to system GND.
(Normal position)</td></tr>
<tr><td>30 ~ 33</td><td>$\overline{\text{AT-0}}$ ~
$\overline{\text{AT-3}}$</td><td>I/O</td><td>—</td><td>Digital attenuator I/O controlled by signal WDCK
WDCK = "L", outputs internal digital attenuator level
WDCK = "H", reads external control data for digital attenuator.
(AT-3 is not connected.)</td><td></td></tr>
<tr><td>34</td><td>$\overline{\text{MUT-1}}$</td><td>I</td><td>—</td><td>Muting control input of the automatic control section of the internal digital attenuator.
At "L", attenuation amount increases (finally, it becomes digital "0"). At "H", attenuation amount decreases (it shifts to 0 dB side).</td><td></td></tr>
<tr><td>35</td><td>$\overline{\text{MUT-01}}$</td><td>O</td><td>—</td><td>Muting 1 output. Outputs an "L" signal when burst error over 64 frames or buffer-over of jitter absorption memory is detected.</td><td></td></tr>
<tr><td>36</td><td>$\overline{\text{MUT-02}}$</td><td>O</td><td>—</td><td>Muting 2 output. Outputs an "L" signal when deinterleave error is detected over 3 continuous frames.</td><td></td></tr>
<tr><td>37</td><td>$\overline{\text{P/S SE}}$</td><td>I</td><td>—</td><td>Output data parallel/serial selection input.
"L" = parallel output, "H" = serial output.</td><td></td></tr>
<tr><td>38</td><td>DA-0</td><td>O</td><td>—</td><td><table><tr><th>P/S SE = "L"</th><th>P/S SE = "H"</th></tr><tr><td>Outputs LSB of 8-bit data.</td><td>Outputs serial data from LSB.</td></tr></table></td><td>Not connected</td></tr>
<tr><td>39</td><td>DA-1</td><td>O</td><td>—</td><td><table><tr><th>P/S SE = "L"</th><th>P/S SE = "H"</th></tr><tr><td>Outputs the second bit from LSB of 8-bit data.</td><td>Outputs correction flag of 8 bits of MSB side.</td></tr></table></td><td>Not connected</td></tr>
<tr><td>40</td><td>DA-2</td><td>O</td><td>—</td><td><table><tr><th>P/S SE = "L"</th><th>P/S SE = "H"</th></tr><tr><td>Outputs the third bit from LSB of 8-bit data.</td><td>Outputs correction flag of 8 bits of LSB side.</td></tr></table></td><td>Not connected</td></tr>
</table>

Table 4-6-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

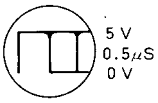
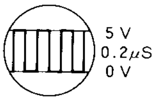
<table>
<tr><th>Pin No.</th><th>Symbol</th><th>I/O</th><th>Waveform</th><th colspan="2">Description</th><th>Remarks</th></tr>
<tr><td>41, 42</td><td>NC</td><td>—</td><td>—</td><td colspan="2">Not connected.</td><td></td></tr>
<tr><td rowspan="2">43</td><td rowspan="2">DA-3</td><td rowspan="2">O</td><td rowspan="2">—</td><td>P/S SE="L"</td><td>P/S SE="H"</td><td rowspan="2">Not connected</td></tr>
<tr><td>Outputs the fourth bit from LSB of 8-bit data.</td><td>Outputs a "H" signal when correction flag of LSB side is set side with level of MSB side at −30 dB.</td></tr>
<tr><td rowspan="2">44</td><td rowspan="2">DA-4</td><td rowspan="2">O</td><td rowspan="2">—</td><td>P/S SE="L"</td><td>P/S SE="H"</td><td rowspan="2">Not connected</td></tr>
<tr><td>Outputs the fifth bit from LSB of 8-bit data.</td><td>1 MCK output.
Outputs the clock signal (1.058 MHz) obtained from 2-division of signal CK2M.</td></tr>
<tr><td rowspan="2">45</td><td rowspan="2">DA-5</td><td rowspan="2">O</td><td rowspan="2">—</td><td>P/S SE="L"</td><td>P/S SE="H"</td><td rowspan="2">Not connected</td></tr>
<tr><td>Outputs the sixth bit from LSB of 8-bit data.</td><td>APL output. Outputs R-channel aperture signal.</td></tr>
<tr><td rowspan="2">46</td><td rowspan="2">DA-6</td><td rowspan="2">O</td><td rowspan="2">—</td><td>P/S SE="L"</td><td>P/S SE="H"</td><td rowspan="2">Not connected</td></tr>
<tr><td>Outputs the seventh bit from LSB of 8-bit data.</td><td>APL output.
Outputs L-channel aperture signal.</td></tr>
<tr><td rowspan="2">47</td><td rowspan="2">DA-7</td><td rowspan="2">O</td><td rowspan="2"> </td><td>P/S SE="L"</td><td>P/S SE="H"</td><td rowspan="2"></td></tr>
<tr><td>Outputs MSB of 8-bit data.</td><td>Outputs music data in serial from MSB.</td></tr>
<tr><td>48</td><td>BCK</td><td>O</td><td> </td><td colspan="2">Bit clock pulse is output when serial data is output. Thus, serial data is output in synchronization with the rising edge of this clock pulse (1.4 MHz).</td><td></td></tr>
</table>

Table 4-6-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

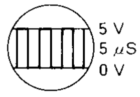
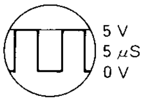
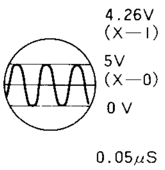
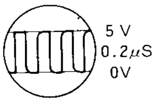
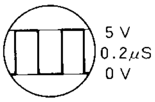
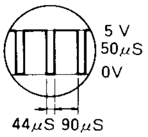
Pin No.	Symbol	I/O	Waveform	Description	Remarks
49	MLCK	O		MSB/LSB clock pulse output. Outputs the clock signal (176.4 kHz) obtained from 8-division of signal BCK, which is used as a set clock pulse when 8-bit parallel data is output.	
50	WDCK	O		Word clock pulse output. Outputs the clock signal (88.2 kHz) obtained from 16-division of signal BCK, which indicates the output period of one word.	
51	L/RG	O		Sampling frequency output. Outputs the clock signal (44.1 kHz) obtained from 2-division of signal WDCK, which indicates the data output channel. "L" = L channel, "H" = R channel.	
52	X-0	O		X'tal OSC connection pins. X'tal OSC is connected to generate the clock signal required in the system. (Feedback resistance and amp incorporated) X'tal OSC frequency = 8.4672 MHz	
53	X-1	I			
54	CKSE	I	—	Selection pin which informs X'tal OSC frequency. (Pullup resistance incorporated) "H" or open = 8.4672 MHz, "L" = 4.2336 MHz	
55	CK4M	O		4 MHz clock pulse output. Outputs 4.2336 MHz, which is also used as the clock signal for microprocessor.	
56	CK2M	O		2 MHz clock pulse output. Outputs 2.1162 MHz, which is used as the clock signal for TC9178AF (IC2).	Connected to C21K (pin 7) of TC9178AF (IC2)
57	TES1	I		Test pins (pullup resistance incorporated) In normal operation, it is "H" or open.	
58	TES2				
59	COFS	O		Frame period signal output. Outputs corrected frame period signal.	

Table 4-6-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

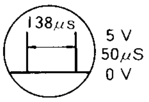
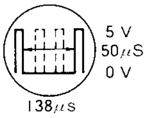
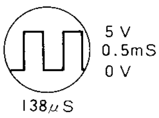
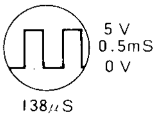
Pin No.	Symbol	I/O	Waveform	Description	Remarks
60	DSLP	O		Data status signal output. (Error information signal output)	
63	DAST	O		Data status signal output. (Error information signal output)	
64	DIV−	O		Buffer memory status output. Outputs an "H" signal when the jitter absorption buffer memory enters range of +2 or +3 frames in its capacity of ±4 frames. This output is connected to pin DIV- of TC9178AF (IC2) to lower the disc motor revolution.	Connected to DIV− (pin 5) of TC9178AF (IC2)
65	DIV+	O		Buffer memory status output. Outputs an "H" signal when the jitter absorption buffer memory enters range of −2 or −3 frames in its capacity of ±4 frames. This output is connected to pin DIV+ of TC9178AF (IC2) to raise the disc motor revolution.	Connected to DIV+ (pin 4) of TC9178AF (IC2)
66	BUSE	I		Buffer selection input pin. Selects the output condition of DIV−/DIV+. At "H", Div± output are made when the buffer memory enters range of ±2 frames. At "L", Div± output are made when it enters range of ±3 frames.	

Table 4-6-1

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-7 PROCESS UNIT: IC3 (HM6116FP-4 or MB8418-20LPF)

- **Abbreviations table**

Symbol	Parameter	Symbol	Parameter
T_{CAC}	Access time from CE2	T_{AA}	Access time from address
T_{OH}	Output hold time from address	T_{WC}	Write cycle time
T_{AAC}	Address access time	T_{AS}	Address set-up time
T_{OD}	Output disable time	T_{AW}	Address write enable time
T_{WP}	Write enable pulse width (Negative)	T_{WR}	Write recovery time
T_{WD}	Write disable pulse width	T_{WHZ}	Output disable time from $R/\overline{W}$
T_{RC}	Read cycle time	T_{WLZ}	Output enable time from $R/\overline{W}$
T_{RS}	Read set-up time	T_{DS}	Data set-up time
T_{RH}	Read hold time	T_{DH}	Data hold time

Table 4-7-1

- **Operation table**

Input			I/O		Operation
$\overline{CE2}$	$R/\overline{W}$	$\overline{CE1}$	DI (Data input)	DO (Data output)	
H	X	X	X	High-Z	Non select
L	H	L	High-Z	DO	Read
L	L	H	DI	High-Z	Write
L	L	L	DI	High-Z	Write
L	H	H	X	High-Z	Select

Table 4-7-2

- **Pin connection**

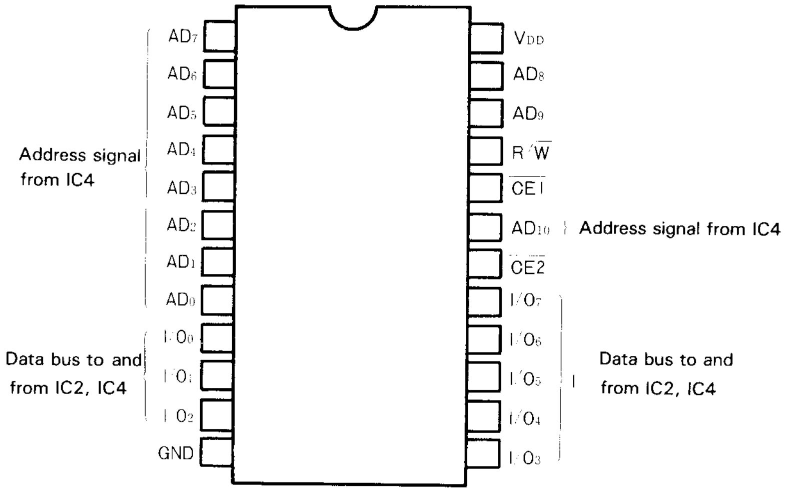

AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
I/O0
I/O1
I/O2
GND
VDD
AD8
AD9
R/W
CE1
AD10
CE2
I/O7
I/O6
I/O5
I/O4
I/O3
Address signal from IC4
Address signal from IC4
Data bus to and from IC2, IC4
Data bus to and from IC2, IC4

Fig. 4-7-1

- **Block diagram**

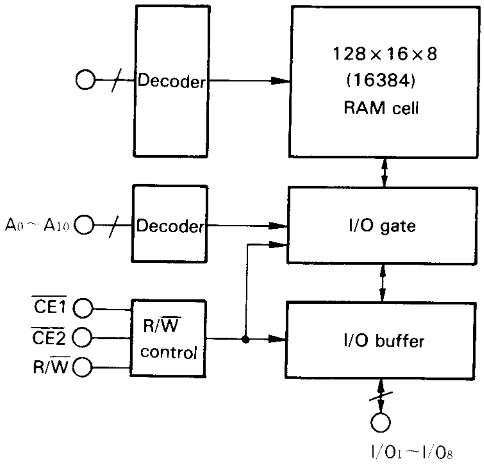

Decoder
128×16×8 (16384) RAM cell
A0~A10
Decoder
I/O gate
CE1
CE2
R/W
R/W control
I/O buffer
I/O1~I/O8

Fig. 4-7-2

- **Waveforms**

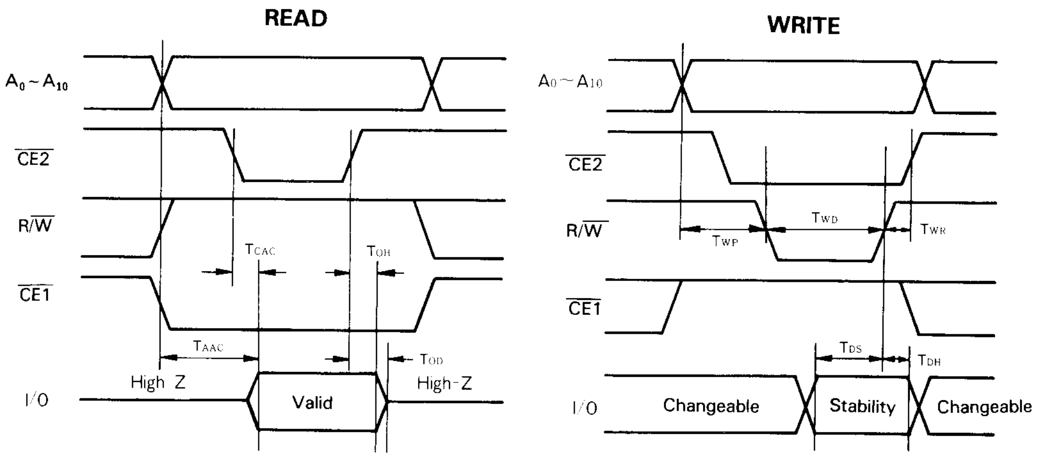

READ
A0~A10
CE2
R/W
CE1
I/O
TCAC
TOH
TAAC
TOD
High Z
Valid
High-Z
WRITE
A0~A10
CE2
R/W
CE1
I/O
TWD
TWP
TWR
TDS
TDH
Changeable
Stability
Changeable

Fig. 4-7-3

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

MODE 1. R/$\overline{W}$ CONTROL ($\overline{CE2}$ = "L", $\overline{CE1}$ = "L")

- **Read cycle**

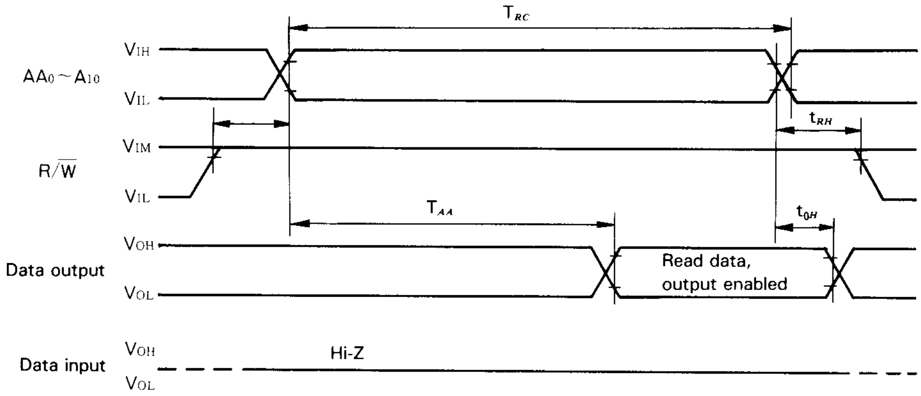

T_{RC}
AA0 ~ A10
VIH
VIL
t_{RH}
R/$\overline{W}$
VIM
VIL
T_{AA}
t_{OH}
Data output
VOH
VOL
Read data, output enabled
Data input
VOH
VOL
Hi-Z

Fig. 4-7-4

- **Write cycle**

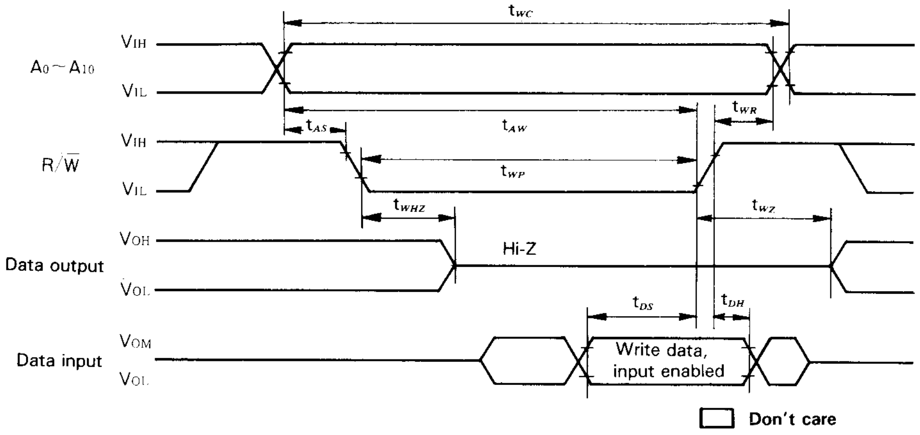

t_{WC}
A0 ~ A10
VIH
VIL
t_{AS}
t_{AW}
t_{WR}
R/$\overline{W}$
VIH
VIL
t_{WP}
t_{WHZ}
t_{WZ}
Data output
VOH
VOL
Hi-Z
t_{DS}
t_{DH}
Data input
VOM
VOL
Write data, input enabled
☐ Don't care

Fig. 4-7-5

MODE3 $\overline{CE1}$ CONTROL ($\overline{CE2}$ = "LO', R/$\overline{W}$ = "H")

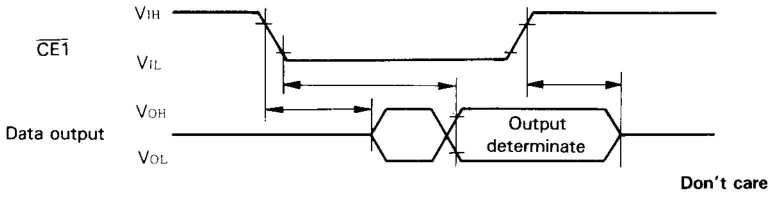
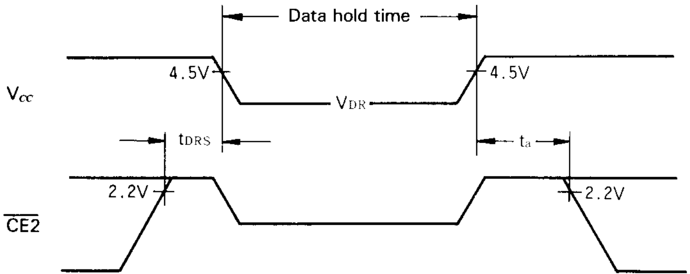

$\overline{CE1}$
VIH
VIL
Data output
VOH
VOL
Output determinate
Don't care

Fig. 4-7-6

Data hold (Condition 1)


Data hold time
V_{cc}
4.5V
VDR
4.5V
tDRS
t_a
2.2V
2.2V
$\overline{CE2}$

•$\overline{CE2}$: 1 When the V_{DR} is from 2.5 to 5.5 volts,
the $\overline{CE2}$ is from 2.2 to V_{DR} +0.3 V.
When the V_{DR} is from 2.0 to 2.5 V,
the $\overline{CE2}$ is from V_{DR} −0.3 to V_{DR}+0.3 V.

Fig. 4-7-7

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-8 D/A CONVERTER: IC11 (CX-20017)

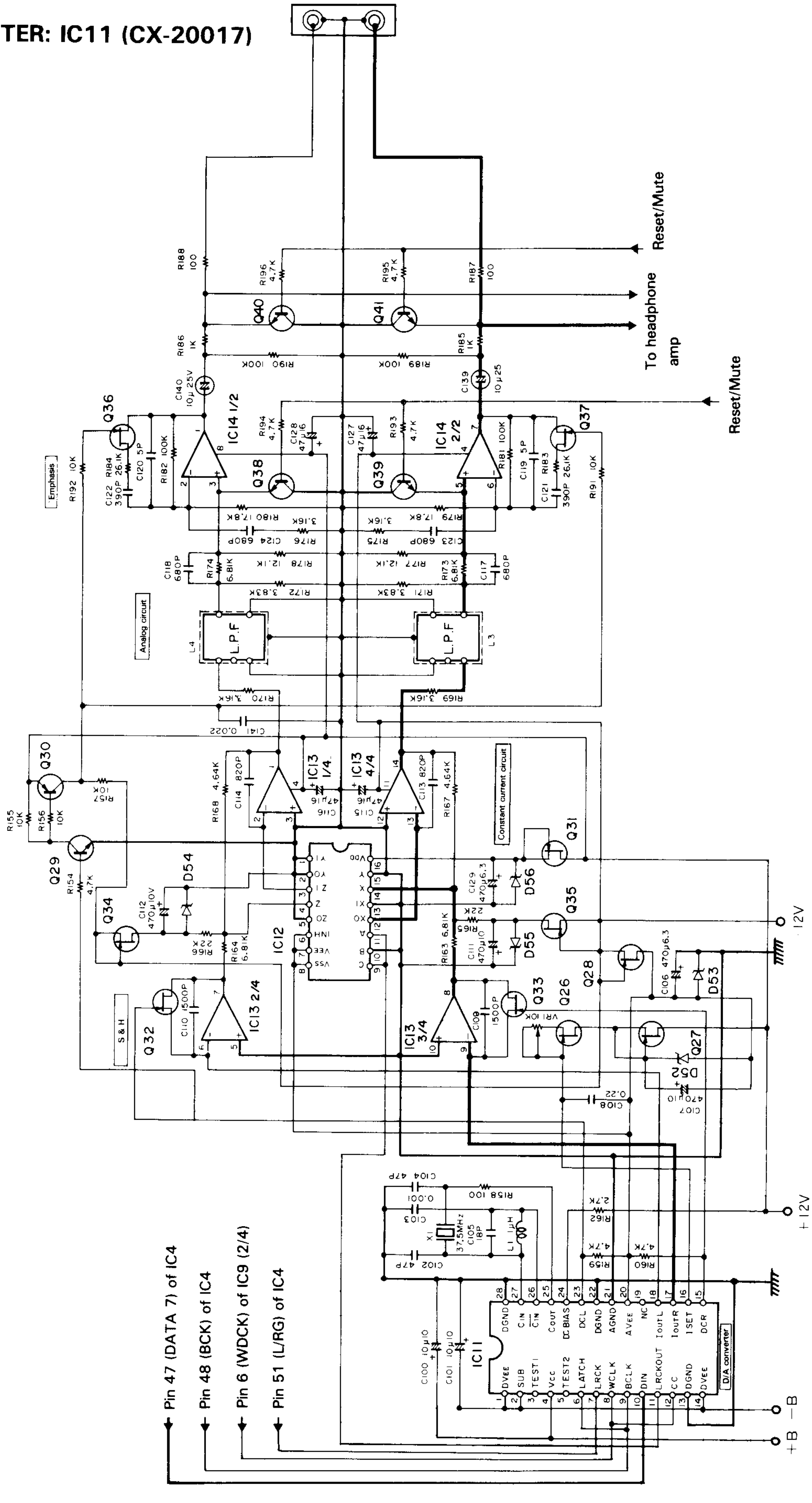
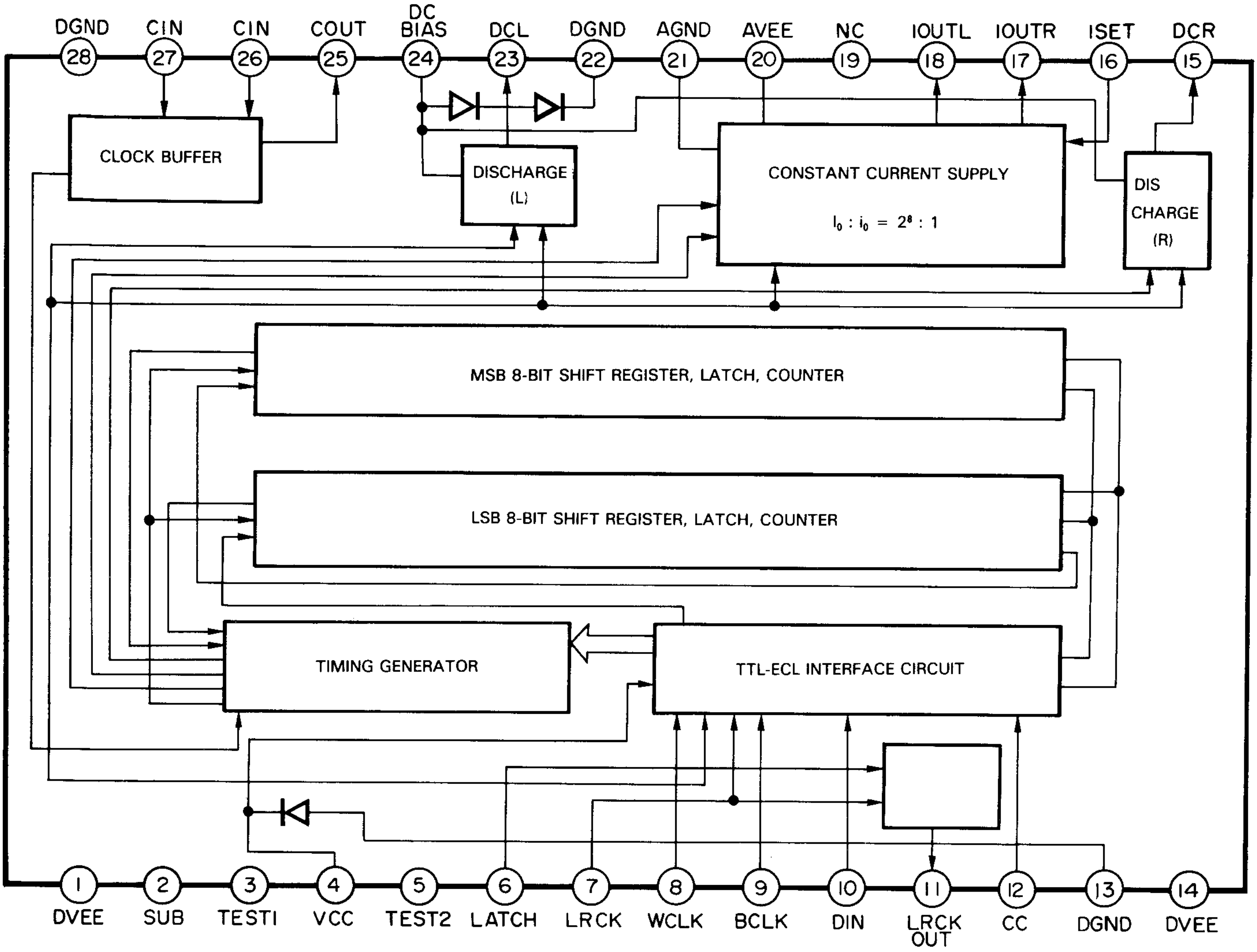

R.CH
L.CH
Reset/Mute
To headphone amp
Reset/Mute
Emphasis
Analog circuit
L.P.F
L.P.F
Constant current circuit
S & H
IC14 1/2
IC14 2/2
IC13 1/4
IC13 4/4
IC13 2/4
IC13 3/4
IC12
IC11
D/A converter
Q29
Q30
Q31
Q32
Q33
Q34
Q35
Q36
Q37
Q38
Q39
Q40
Q41
Q26
Q27
Q28
D52
D53
D54
D55
D56
12V
+12V
+B
−B
Pin 47 (DATA 7) of IC4
Pin 48 (BCK) of IC4
Pin 6 (WDCK) of IC9 (2/4)
Pin 51 (L/RG) of IC4

Fig. 4-8-1 Circumference circuit of the CX-20017

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

Block diagram


DGND
CIN
CIN
COUT
DC BIAS
DCL
DGND
AGND
AVEE
NC
IOUTL
IOUTR
ISET
DCR
28
27
26
25
24
23
22
21
20
19
18
17
16
15
CLOCK BUFFER
DISCHARGE (L)
CONSTANT CURRENT SUPPLY
$I_0 : i_0 = 2^8 : 1$
DIS CHARGE (R)
MSB 8-BIT SHIFT REGISTER, LATCH, COUNTER
LSB 8-BIT SHIFT REGISTER, LATCH, COUNTER
TIMING GENERATOR
TTL-ECL INTERFACE CIRCUIT
1
2
3
4
5
6
7
8
9
10
11
12
13
14
DVEE
SUB
TEST1
VCC
TEST2
LATCH
LRCK
WCLK
BCLK
DIN
LRCK OUT
CC
DGND
DVEE

Uses the TEST1 and TEST2 are open.

Fig. 4-8-2 IC11 (CX-20017) Block diagram

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

CONVERSION OPERATION OF IC11 (CX-20017)

(1) Data calling (BCLK, DIN, WCLK and LRCK)

The data is a 16-bit serial signal and takes the format of the 2's complement. The data is sent from MSB into the IC sequentially synchronized with the leading edge of the bit clock (BCLK). (The data changes at the trailing edge of BCLK.)

When the work clock (WCLK) is changed from high to low level at the trailing edge of 17th BCLK, the 16-bit data is transferred from the shift register to the latch by this trailing signal. In the case of using CX-20017 in the stereo mode, the data of another channel is sent from the 17th BCLK on.

As for the data allocation in the stereo mode, the R-channel data is called when LRCK is at the "L" level, and the L-channel data is called when it is at the "H" level.

IOUTL and DCL work when the level of LRCK is low, while IOUTR and DCR work when the level is high.

(2) Conversion operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL and DCR)

When the conversion command (CC) is set to high level and more than three clocks are entered from the clock input (CIN), all internal timing circuits are reset. After these circuits are reset, when the CC is set to low level and a clock is entered from the CIN, the internal timing circuits start operation. The signals generated thereby are a discharge signal, a counter set signal and an integration current start signal. The durations of these three signals are determined as shown below by the clock cycle and quantity.

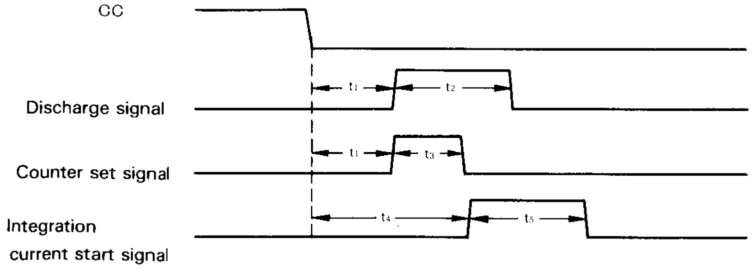


Fig. 4-8-3

$t_1 = 34 \times \tau 0$

$t_2 = 67 \times \tau 0$

$t_3 = 31 \times \tau 0$

$t_4 = 65 \times \tau 0$

$t_5\text{min} = 47 \times \tau 0$ (Input data 01 ~ 1)

$t_5\text{max} = 302 \times \tau 0$ (Input data 10 ~ 0)

The counter set signal is used to set the data applied to the latch in the counter, which is not output externally. The discharge signal is output from DCL DCR: it is output from DCL when the LRCK level is low and from DCR when the level is high.

When the integration current start signal, the high-order current I_0 and low-order current i_0 start to flow.

The counter starts counting from the preset value as soon as the discharge signal is turned off, and it outputs the signal used to stop the integration current.

The value of t_5 is changed in the range of 0 ~ 255 by the input data value preset in the counter.

Thus, the time from the timing that the CC goes to low level to the end of integration, that is, the conversion time, requires ($t_4 + t_5$ max.) seconds maximum.

This integration current is output as IOUTL when the LRCK level is low and IOUTR when it is high just like the discharge signal.

(3) Setting of integration current (ISET, IOUTL and IOUTR)

The integration current is determined by the constant current value flowing from the ISET terminal. The relation between them is as follows:

$$\text{IOUTL (R)} = I_0 + i_0 = \left(4 + \frac{1}{64}\right) \text{ISET}$$

The "i_0" indicates the integration current corresponding to 1LSB and "I_0" the integration current corresponding 2^8·LSB.

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

(4) Operation of LRCK OUT (LATCH, LRCK and LRCK OUT)

The output of LRCK OUT is used to drive the analog switch IC12 (MPD14053BC) which takes the output converted by CX-20017 and integrator as a PAM waveform.

When the PAM waveform includes a jitter, it causes a conversion error. The D-type flip-flop is provided to absorb the jitter. The LATCH input is used as a clock for this. The D-type flip-flop synchronizes with the leading edge of the clock and change the output state. The LRCK OUT works only when +5 V is applied to VCC. The output voltage level is −3 V to +3 V.

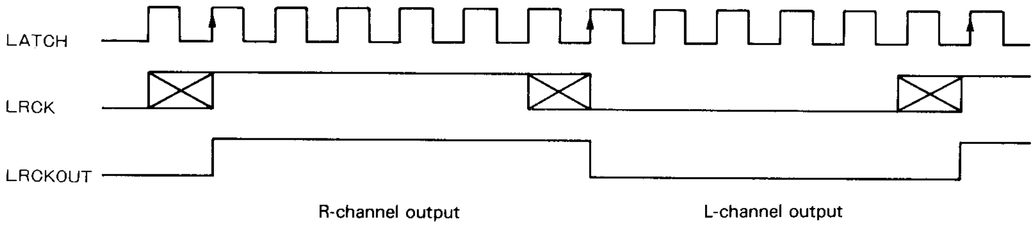


Fig. 4-8-4 Timing of LATCH, LRCK and LRCK OUT

(5) Clock input/output terminals (COUT, CIN and $\overline{\text{CIN}}$)

The clock buffer consists of a general purpose ECL logic circuit and an equivalent circuit. The input terminal is biassed by the internal bias circuit. (≈ −1.3 V) The output amplitude level is 0.8 V.

(6) Bias terminals (DVEE, SUB, DGND, VCC, AVEE, AGND and DC BIAS)

SUB is the substrate of the IC and used at a common potential with DVEE. The standard values of DVEE and AVEE are −5.0 V. In the CX-20017, the VCC terminal is raised to +5 V in order to operate the input in the range of 0 to +5 V. As described before, LRCK OUT is output in this case. DC BIAS is the bias circuit of the output circuit for the discharge signal.

As it requires a current of about 2.5 mA as a standard value, the power is supplied from IC15. The potential of this terminal is biassed to 2vf.

4. IC OPERATION OF EACH CIRCUIT AND PIN DESCRIPTION

4-9 CMOS INTEGRATED CIRCUIT: IC2 (μPD4053BC)

Pin connection

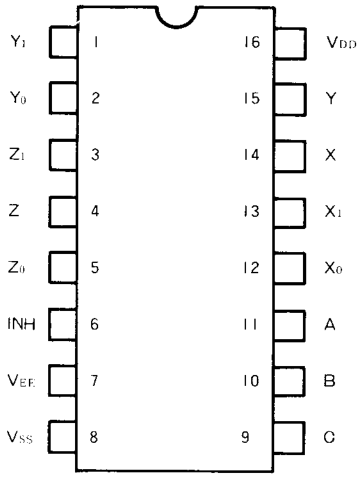

Y1 1
Y0 2
Z1 3
Z 4
Z0 5
INH 6
VEE 7
VSS 8
16 VDD
15 Y
14 X
13 X1
12 X0
11 A
10 B
9 C

Fig. 4-9-1
(Top view)

Truth table

Control input				"ON" channel
INHIBIT	C	B	A	
L	L	L	L	Z_0, Y_0, X_0
L	L	L	H	Z_0, Y_0, X_1
L	L	H	L	Z_0, Y_1, X_0
L	L	H	H	Z_0, Y_1, X_1
L	H	L	L	Z_1, Y_0, X_0
L	H	L	H	Z_1, Y_0, X_1
L	H	H	L	Z_1, Y_1, X_0
L	H	H	H	Z_1, Y_1, X_1
H	X	X	X	None

H: High level
L: Low level
X: H or L
B: Fixed to "L"

Table 4-9-1

Block diagram

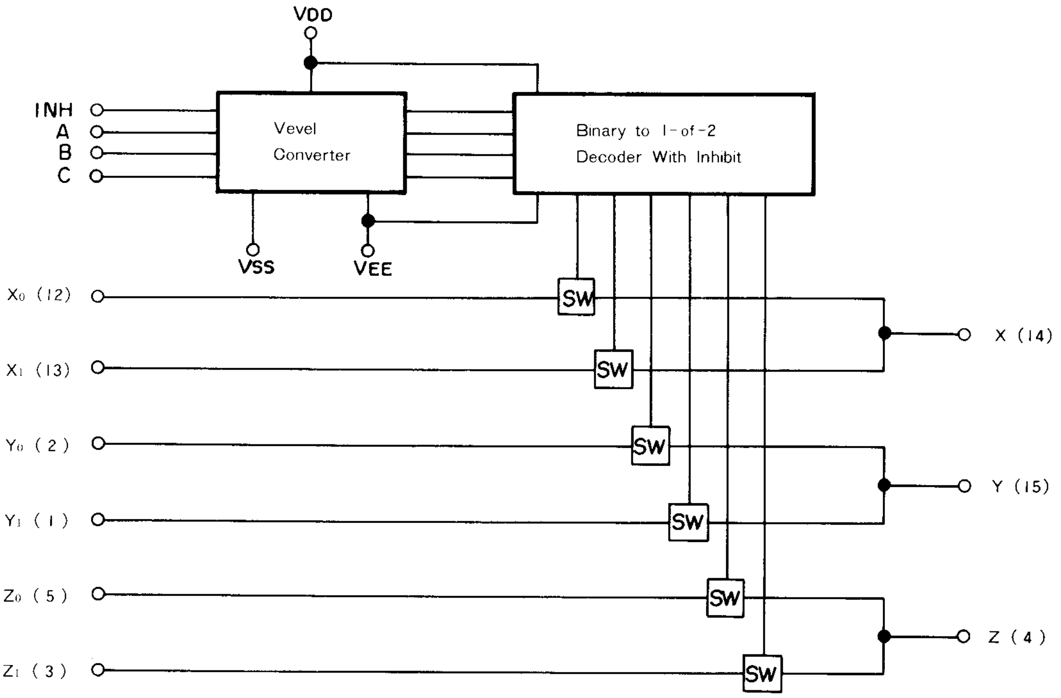

VDD
INH
A
B
C
Vevel Converter
Binary to 1-of-2 Decoder With Inhibit
VSS
VEE
X0 (12)
X1 (13)
Y0 (2)
Y1 (1)
Z0 (5)
Z1 (3)
SW
SW
SW
SW
SW
SW
X (14)
Y (15)
Z (4)

Fig. 4-9-2

5. TROUBLESHOOTING

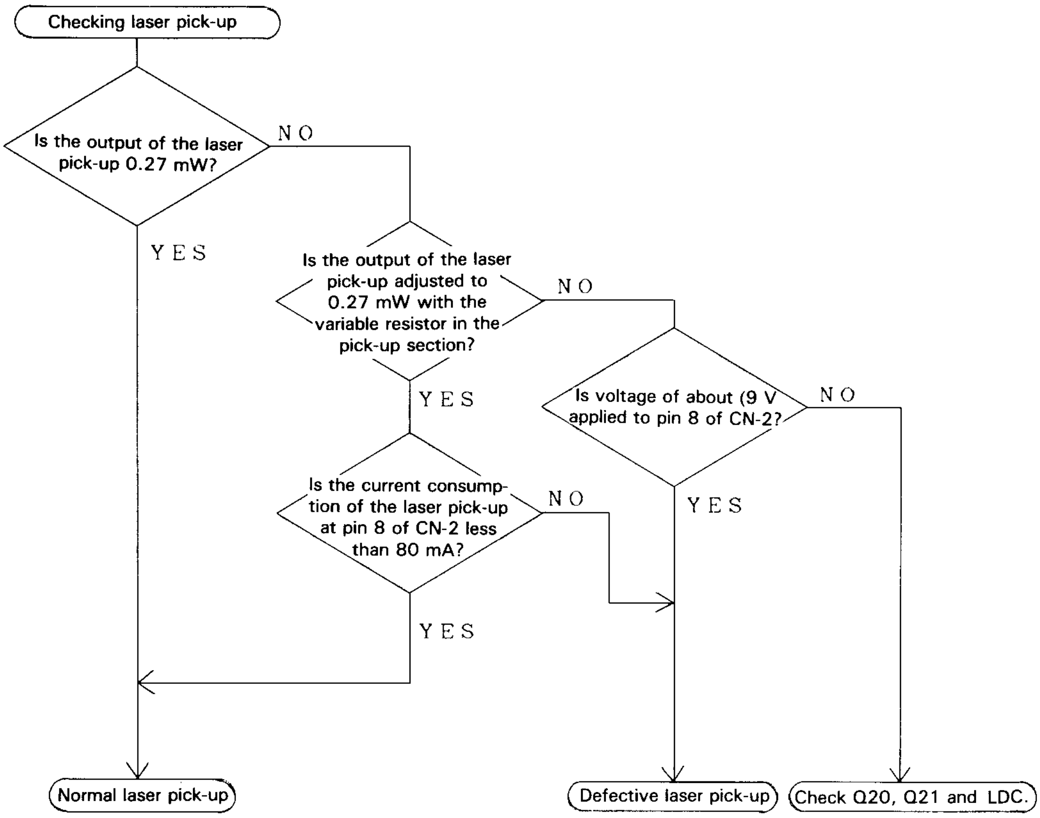

Checking laser pick-up
Is the output of the laser pick-up 0.27 mW?
NO
YES
Is the output of the laser pick-up adjusted to 0.27 mW with the variable resistor in the pick-up section?
NO
YES
Is voltage of about (9 V applied to pin 8 of CN-2?
NO
YES
Is the current consumption of the laser pick-up at pin 8 of CN-2 less than 80 mA?
NO
YES
Normal laser pick-up
Defective laser pick-up
Check Q20, Q21 and LDC.

Fig. 5

6. ADJUSTMENT

No.	ITEM	INPUT SETTINGS	OUTPUT SETTINGS	PLAYER SETTINGS	ALIGNMENT POINTS	ALIGN FOR	FIG.
1	LASER POWER	–	Set a laser power meter on the pickup.	(X29-1600-11) Short-circuit TP17 and 18.	Pickup section VR	0.27mW	(a)
2	LASER OPERATION CURRENT CHECK (only when pickup appears to malfunction)	–	(X29-1600-11) Remove CN2 pin 8 and connect the DC current meter.	(X29-1600-11) Short-circuit TP17 and 18.	–	Current displayed with pickup shall be below 80mA.	(b)
Following items are adjusted when replacing the pickup.							
3	FOCUS ERROR BALANCE	Test disc	(X29-1610-00) Connect an oscilloscope at TP2.	(X29-1600-11) Release the short circuit of TP17 and 18. PLAY	(X29-1610-00) VR2	Best eye pattern	(c)
4	TANGENTIAL	Test disc	(X29-1610-00) Connect an oscilloscope at TP2.	PLAY	Hex screw below the mechanism	Best eye pattern	(d)
5	PICKUP (diffraction grating) (1)	Test disc	(X29-1610-00) Connect an oscilloscope at TP3.	(X29-1600-11) While short-circuiting TP15 and 16, switch the power from OFF to ON, search the first tune(about 2:00)with the UP/DOWN key which sets the microprocessor to test mode, and press the PAUSE key.	Pickup adjustment hole (W05-0064-00) Use a grid driver.	Max.amplitude	(e)
6	PICKUP (diffraction grating) (2)	Test disc	(X29-1610-00) Connect an oscilloscope at TP2.	PLAY	Pickup adjustment hole	Best eye pattern	
7	PICKUP (diffraction grating) (3)	Test disc	(X29-1610-00) Connect an oscilloscope at TP5 and trigger with TP2.	PLAY	Pickup adjustment hole	Photo A	(f)
8	TRACKING ERROR BALANCE	Test disc	(X29-1610-00) Connect an oscilloscope or tester at TP3.	PAUSE (condition of 3)	(X29-1610-00) VR3	0V±0.1V	(g)
9	FOCUS GAIN	(X29-1610-00) Apply 1kHz, 50mV signal to CN2 pin 2.	(X29-1610-00) Connect a 47kΩ, 470PF LPF to CN2 pin 1, then connect an oscilloscope or AC voltmeter.	Switch power from OFF to ON and set the microprocessor in normal condition. PLAY	(X29-1610-00) VR4	50mV	(h)
10	TRACKING GAIN	(X29-1600-11) Apply 1.5kHz, 50mV signal to CN3 pin 2.	(X29-1600-11) Connect a 47kΩ, 470PF LPF to CN3 pin 1, then connect an oscilloscope or AC voltmeter.	(X29-1600-11) Short-circuit TP11 and 12 so that dropout control does not function. PLAY	(X29-1610-00) VR1	50mV	(i)
11	CLAMPER HEIGHT	–	Clearance between clamper and clamper arm.	Withdraw the tray without loading a disc.	Clamper height adjustment screw.	0.5mm	(j)
12	PLL	Test disc	(X32-1020-00) Connect a DC voltmeter to the cathode of D1.	PLAY	(X32-1020-00) L1	5V	(k)
13	OUTPUT VOLTAGE	Test disc (1kHz,0dB)	Connect an AC voltmeter to OUTPUT.	PLAY	(X29-1600-11) VR1	2V	(l)

6. REGLAGE

N°	ITEM	REGLAGE DE L'ENTREE	REGLAGE DE LA SORTIE	REGLAGE DE LA LECTURE	POINT DE L'ALIGNEMENT	ALIGNER POUR	FIG.
1	ALIMENTATION LASER	–	Placer un appareil de mesure de puissance de laser sur le capteur.	(X29-1600-11) Court-circuiter TP17 et 18.	VR de la section capteur.	0,27mW	(a)
2	VERIFICATION DE TENSION DE FONCTIONNEMENT DU LASER (seulement si le capteur semble mal fonctionner)	–	(X29-1600-11) Enlever la broche 8 de CN2 et connecter l'ampèremètre CC.	(X29-1600-11) Court-circuiter TP17 et 18.	–	Le courant affiché au niveau du capteur doit être inférieur à 80mA.	(b)
Les éléments suivants se réglent lors du remplacement du capteur.							
3	EQUILIBRE D'ERREUR DE FOCALISATION	Disque test	(X29-1610-00) Connecter un oscilloscope à TP2.	(X29-1600-11) Défaire le court-circuit entre TP17 et 18. Passer en lecture(PLAY).	(X29-1610-00) VR2	Meilleur motif à l'oeil.	(c)
4	TANGENTIEL	Disque test	(X29-1610-00) Connecter un oscilloscope à TP2.	PLAY	Vis à six pans sous le mécanisume.	Meilleir motif à l'oeil.	(d)
5	CAPTEUR (réseau de diffraction) (1)	Disque test	(X29-1610-00) Connecter un oscilloscope à TP3.	(X29-1600-11) En court-circuitant TP15 et 16, commuter l'alimentation de OFF à ON, rechercher le premier morceau (à environ 2:00) avec la touche UP/DOWN qui met le microprocesseur en mode test, puis appuyer sur la touche PAUSE.	Orifice de réglage du capteur (W05-0064-00) Utiliser un tournevis de grille.	Amplitude max.	(e)
6	CAPTEUR (réseau de diffraction) (2)	Disque test	(X29-1610-00) Connecter un oscilloscope à TP2.	PLAY	Orifice de réglage du capteur.	Meilleur motif à l'oeil.	
7	CAPTEUR (réseau de diffraction) (3)	Disque test	(X29-1610-00) Connecter un oscilloscope à TP5 et déclencher avec TP2.	PLAY	Orifice de réglage du capteur.	Photo A	(f)
8	EQUILIBRE D'ERREUR D'ALIGNEMENT	Disque test	(X29-1610-00) Connecter un oscilloscope ou un testeur à TP3.	PAUSE (condition de 3)	(X29-1610-00) VR3	0V±0,1V	(g)
9	GAIN DE FOCALISATION	(X29-1610-00) Envoyer un signal de 1kHz,50mV à la broche 2 de CN2.	(X29-1610-00) Connecter un LPF de 47kΩ, 470PF à la broche 1 de CN2, puis connecter un oscilloscope ou un voltmètre CA.	Commuter l'alimentation de OFF à ON et mettre le microprocesseur en état normal. Passer en lecture (PLAY).	(X29-1610-00) VR4	50mV	(h)
10	GAIN D'ALIGNEMENT	(X29-1600-11) Envoyer un signal de 1,5kHz,50mV à la broche 2 de CN3.	(X29-1600-11) Connecter un LPF de 47kΩ, 470PF à la broche 1 de CN3, puis connecter un oscilloscope ou un voltmètre CA.	(X29-1600-11) Court-circuiter TP11 et 12 de telle sorte que la commande de désexcitation ne fonctionne plus. Passer en lecture(PLAY).	(X29-1610-00) VR1	50mV	(i)
11	HAUTEUR DE COUPLEUR	–	Dégagement entre le coupleur et son bras.	Reculer le plateau sans charger de disque.	Vis de réglage de hauteur du coupleur.	0,5mm	(j)
12	PLL	Disque test	(X32-1020-00) Connecter un voltmètre CC à la cathode de D1.	PLAY	(X32-1020-00) L1	5V	(k)
13	TENSION DE SORTIE	Disque test (1kHz,0dB)	Connecter un voltmètre CA à OUTPUT.	PLAY	(X29-1600-11) VR1	2V	(l)

6. ABGLEICH

NR.	GEGENSTAND	EINGANGS-EINSTELLUNG	AUSGANGS-EINSTELLUNG	SPIELER-EINSTELLUNG	ABGLEICH-PUNKTE	ABGLEICHEN FÜR	ABB.
1	LASERLEISTUNG	—	Ein Laserleistung-Meßgerät an den Aufnehmer stellen.	(X29-1600-11) TP17 und 18 kurzschließen.	Aufnehmer-abschnitt VR	0,27mW	(a)
2	PRÜFUNG DES LASER-BETRIEBSSTROMS (nur wenn der Aufnehmer Störungen zu haben scheint)	—	(X29-1600-11) CN2 Stift 8 entfernen und den Gleichstrom-Meter anschließen.	(X29-1600-00) TP17 und 18 kurzschließen.	—	Der mit dem Aufnehmer angezeigte Strom muß unter 80mA sein.	(b)
Beim Auswechseln des Aufnehmers müssen die folgenden Punkte eingestellt werden.							
3	FOKUSSIER-FEHLER-BALANCE	Testplatte	(X29-1610-00) Ein Oszilloskop an TP2 anschließen.	(X29-1600-11) Den Kurzschluß von TP17 und 18 aufheben. PLAY	(X29-1610-00) VR2	Bestes Augenmuster	(c)
4	TANGENTIAL	Testplatte	(X29-1610-00) Ein Oszilloskop an TP2 anschließen.	PLAY	Sechskantschraube unter dem Mechanismus	Bestes Augenmuster	(d)
5	AUFNEHMER (Beugungsgitter) (1)	Testplatte	(X29-1610-00) Ein Oszilloskop an TP3 anschließen.	(X29-1600-11) Während TP15 und 16 kurzgeschlossen sind, die Spannungsversorgung von OFF auf ON schalten, mit der UP/DOWN-Taste, die den Mikroprozessor auf den Testmodus stellt, das erste Stück suchen (etwa 2:00) und die PAUSE-Taste drücken.	Aufnehmer-Einstellöffnung (W05-0064-00) Einen Gitter-Treiber verwenden.	Max. Amplitude	(e)
6	AUFNEHMER (Beugungsgitter) (2)	Testplatte	(X29-1610-00) Ein Oszilloskop an TP2 anschließen.	PLAY	Aufnehmer-Einstellöffnung	Bestes Augenmuster	
7	AUFNEHMER (Beugungsgitter) (3)	Testplatte	(X29-1610-00) Ein Oszilloskop an TP5 anschließen und mit TP2 auslösen.	PLAY	Aufnehmer-Einstellöffnung	Foto A	(f)
8	SPURHALTE-FEHLER-BALANCE	Testplatte	(X29-1610-00) Ein Oszilloskop oder einen Tester an TP3 anschließen.	PAUSE (Bedingung von 3)	(X29-1610-00) VR3	0V±0,1V	(g)
9	ERNEUT FOKUSSIEREN	(X29-1610-00) Ein 1kHz, 50mV Signal an CN2 Stift 2 anlegen.	(X29-1610-00) Einen 47kΩ, 470PF Tiefpaßfilter an CN2 Stift 1 anschließen und dann ein Oszilloskop oder einen Wechselstrom-Voltmeter anschließen.	Die Spannungsversorgung von OFF auf ON schalten und den Mikroprozessor in den normalen Zustand stellen. PLAY	(X29-1610-00) VR4	50mV	(h)
10	SPURHALTE-VERSTÄRKUNG	(X29-1600-11) Ein 1,5kHz, 50mV Signal an CN3 Stift 2 anlegen.	(X29-1600-11) Einen 47kΩ, 470PF Tiefpaßfilter an CN3 Stift 1 anschließen und dann ein Oszilloskop oder einen Wechselstrom-Voltmeter anschließen.	(X29-1600-11) TP11 und 12 kurzschließen, so daß die Ausfallkontrolle nicht arbeitet. PLAY	(X29-1610-00) VR1	50mV	(i)
11	BEFESTIGER-HÖHE	—	Freiraum zwischen Befestiger und Befestigerarm	Die Schublade zurückziehen, ohne eine Platte zu laden.	Einstellschraube für Befestiger-Höhe	0,5mm	(j)
12	PLL	Testplatte	(X32-1020-00) Einen Gleichstrom-Voltmeter an die Kathode von D1 anschließen.	PLAY	(X32-1020-00) L1	5V	(k)
13	AUSGANGS-SPANNUNG	Testplatte (1kHz,0dB)	Einen Wechselstrom-Voltmeter an OUTPUT anschließen.	PLAY	(X29-1600-11) VR1	2V	(l)

6-1. ADJUSTMENT POINT

6-1-1. Adjustment points of CN2, 3

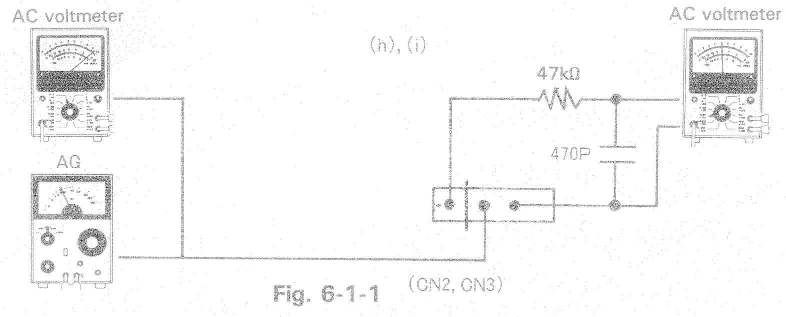

AC voltmeter
AG
(h), (i)
47kΩ
470P
AC voltmeter
(CN2, CN3)

Fig. 6-1-1

6-1-2. Adjustment points of top side view

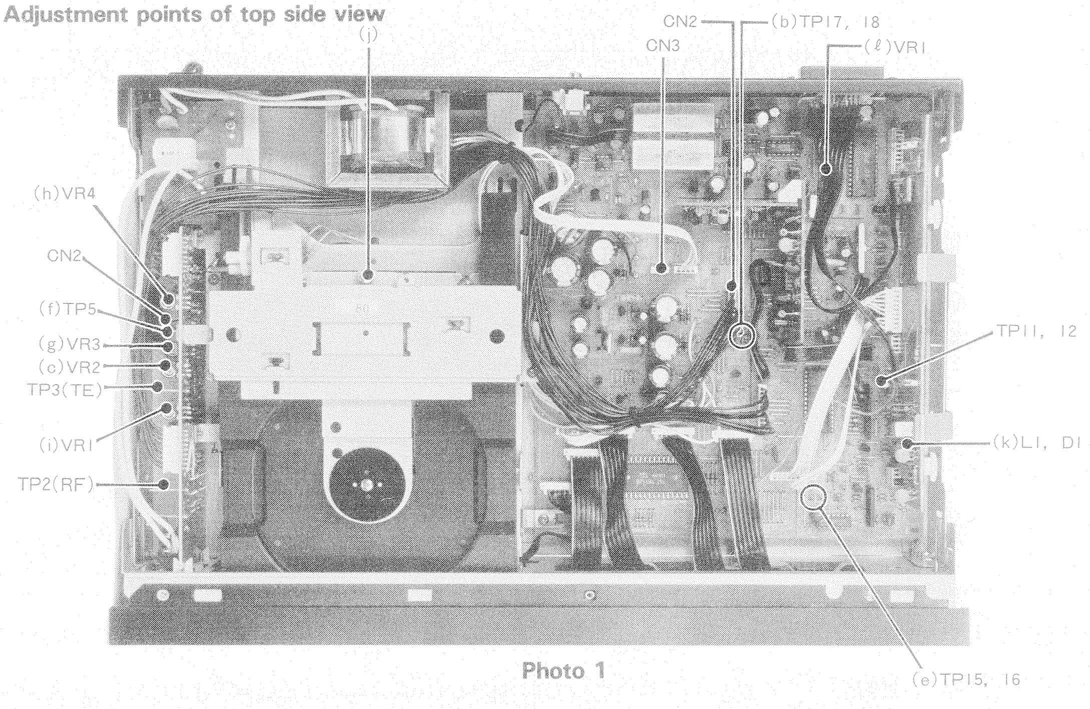

(j)
CN2
(b)TP17, 18
CN3
(ℓ)VR1
(h)VR4
CN2
(f)TP5
(g)VR3
(c)VR2
TP3(TE)
(i)VR1
TP2(RF)
TP11, 12
(k)L1, D1
(e)TP15, 16

Photo 1

6-1-3. Adjustment points of bottom side view

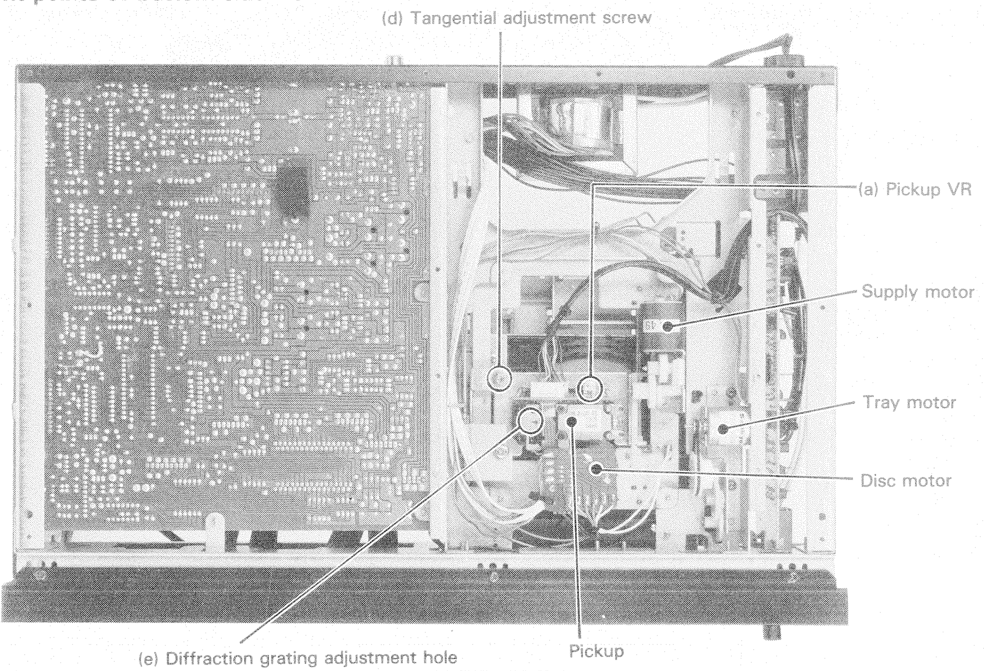
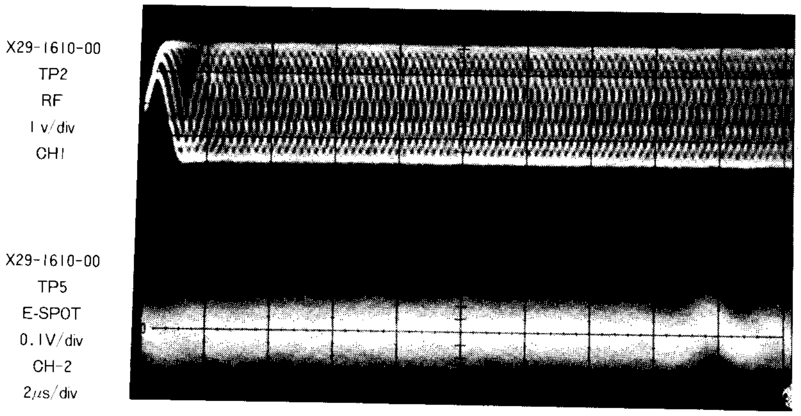

(d) Tangential adjustment screw
(a) Pickup VR
Supply motor
Tray motor
Disc motor
(e) Diffraction grating adjustment hole
Pickup

Photo 2

6-1-4. Waveform test points



Waveform at this point is important.

Photo 3

6-2. TRACKING ERROR BALANCE

TE-BAL, VR3 (X29-1610-00)

Set for the focus servo ON and tracking servo OFF (see item (3)) and observe test pin 3 (TE) of X29-1610-00. Adjust so that the TETE waveform is symmetrical above and below 0 V DC. If available, connect an analog DC voltage and adjust to within ±0.1 V.

6-3. Focus gain

F-GAIN, VR4 (X29-1610-00)

Apply a 1 kHz, 50 mV rms signal to pin 2 of CN2 of X29-1610-00. Connect an LPF consisting of 47 kilohm R and 470 pF C and adjust so that the output level is the same as the signal applied to pin 2 (i.e. 50 mV rms). Because noise is also included at this time, adjust paying attention only to the same frequency component. When using an AC meter, use an average value detection type meter.

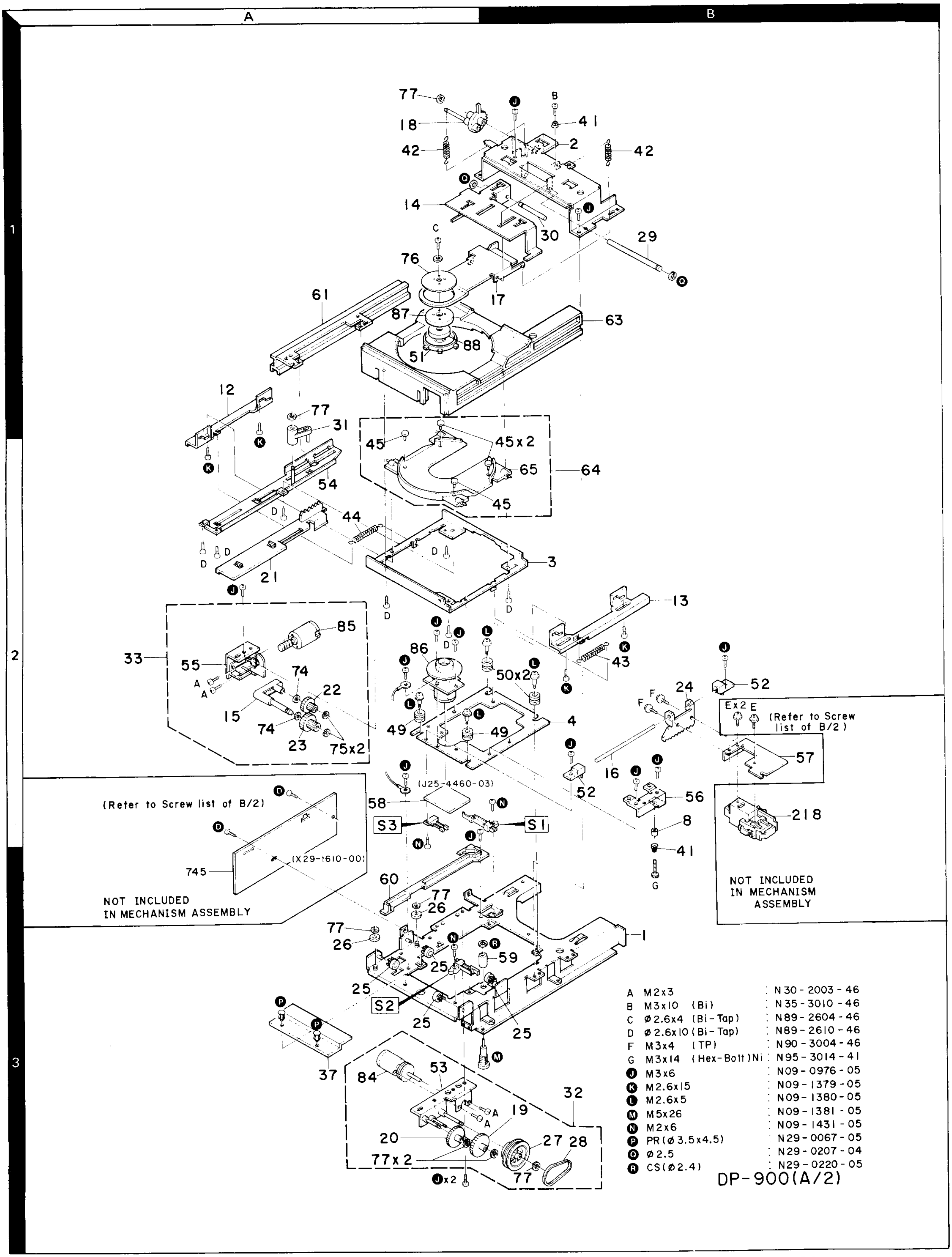
6-4. Tracking gain

T-GAIN, VR1 (X29-1610-00)

The adjustment is almost the same as the focus gain adjustment. However, the connection is made to CN3 of X29-1610-00 instead of CN2 of X29-1610-90, and the applied signal is 1.5 kHz, 50 mV rms signal. As the adjustment could be erroneous when the dropout control is operating, test pins 11 and 12 of X29-1600-00 should be short-circuited to deactivate the dropout control.

7. EXPLODED VIEW

7-1. MECHANISM UNIT

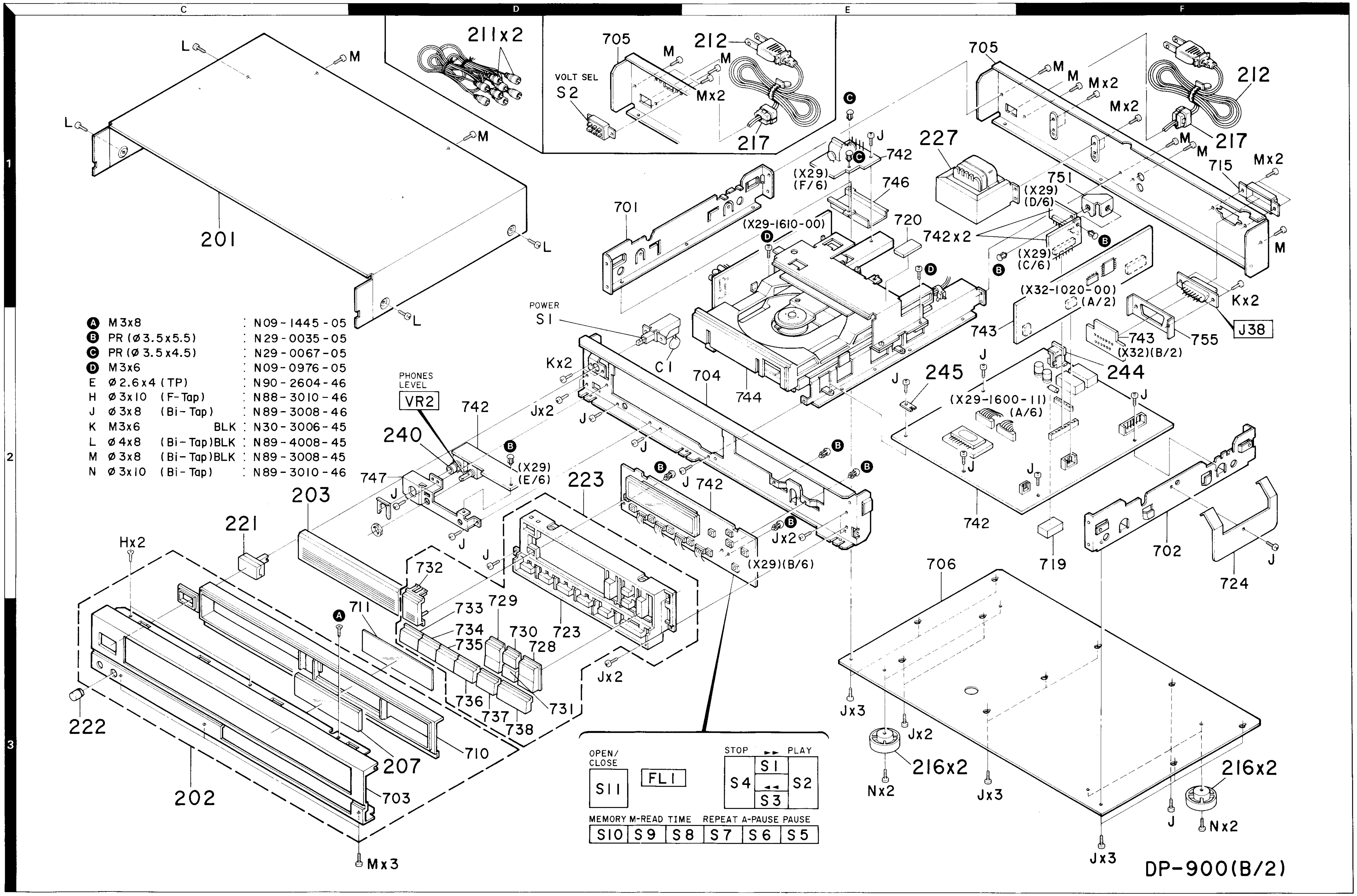

A
B
1
2
3
77
18
42
J
B
41
2
42
Q
14
J
30
29
C
76
Q
17
61
87
63
51
88
12
77
31
K
K
45
45x2
65
64
54
45
D
44
D
D D
D
3
21
J
D
D
13
33
85
J
J
D
L
55
86
J
L
K
A
74
43
A
22
J
50x2
K
J
15
24
52
74
L
F
49
23
75x2
49
4
F
Ex2 E
(Refer to Screw list of B/2)
57
J
J
16
J
(J25-4460-03)
52
J
56
(Refer to Screw list of B/2)
D
58
N
S3
S1
8
218
D
N
J
41
(X29-1610-00)
745
G
60
NOT INCLUDED IN MECHANISM ASSEMBLY
NOT INCLUDED IN MECHANISM ASSEMBLY
77
26
77
26
N
R
L
59
25
1
25
S2
P
25
25
P
M
37
84
53
32
A
19
A
20
27
28
77x2
Jx2
77
DP-900(A/2)

A	M2x3	N30-2003-46
B	M3x10 (Bi)	N35-3010-46
C	ø2.6x4 (Bi-Tap)	N89-2604-46
D	ø2.6x10 (Bi-Tap)	N89-2610-46
F	M3x4 (TP)	N90-3004-46
G	M3x14 (Hex-Bolt)Ni	N95-3014-41
J	M3x6	N09-0976-05
K	M2.6x15	N09-1379-05
L	M2.6x5	N09-1380-05
M	M5x26	N09-1381-05
N	M2x6	N09-1431-05
P	PR(ø3.5x4.5)	N29-0067-05
Q	ø2.5	N29-0207-04
R	CS(ø2.4)	N29-0220-05

Parts with the exploded numbers larger than 700 are not supplied.

7. EXPLODED VIEW

7-2. MAIN UNIT


C
D
E
F
1
2
3
L
M
L
M
201
L
L
211x2
VOLT SEL
S2
705
M
212
M
Mx2
217
701
(X29)
(F/6)
742
J
746
720
(X29-1610-00)
742x2
227
751
(X29)
(D/6)
(X29)
(C/6)
705
M
M
Mx2
Mx2
M
M
212
217
715
Mx2
M
(X32-1020-00)
(A/2)
743
743
(X32)(B/2)
755
Kx2
J38
POWER
S1
C1
Kx2
704
744
Jx2
J
245
J
244
(X29-1600-11)
(A/6)
PHONES
LEVEL
VR2
742
240
(X29)
(E/6)
747
J
J
203
223
J
742
Jx2
(X29)(B/6)
J
742
702
724
J
719
706
221
Hx2
732
733
734
735
729
730
728
723
Jx2
711
736
737
738
731
222
207
710
202
703
Mx3
OPEN/
CLOSE
S11
FL1
STOP
►►
PLAY
S1
S4
S2
◄◄
S3
MEMORY M-READ TIME REPEAT A-PAUSE PAUSE
S10
S9
S8
S7
S6
S5
Jx3
Jx2
216x2
Nx2
Jx3
216x2
J
Nx2
Jx3
DP-900(B/2)

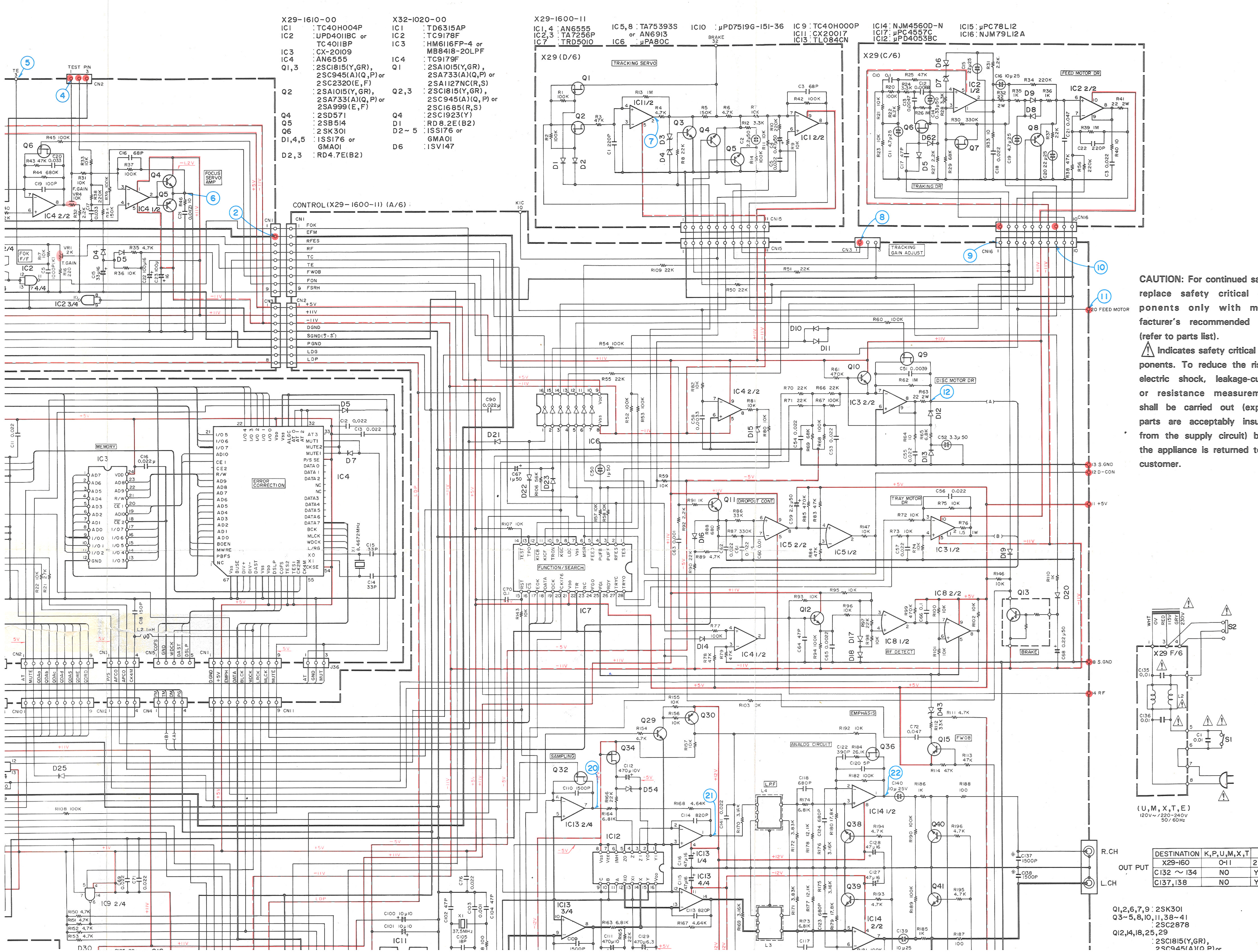
Ⓐ	M3x8		N09-1445-05
Ⓑ	PR (Ø3.5x5.5)		N29-0035-05
Ⓒ	PR (Ø3.5x4.5)		N29-0067-05
Ⓓ	M3x6		N09-0976-05
E	Ø2.6x4 (TP)		N90-2604-46
H	Ø3x10	(F-Tap)	N88-3010-46
J	Ø3x8	(Bi-Tap)	N89-3008-46
K	M3x6	BLK	N30-3006-45
L	Ø4x8	(Bi-Tap)BLK	N89-4008-45
M	Ø3x8	(Bi-Tap)BLK	N89-3008-45
N	Ø3x10	(Bi-Tap)	N89-3010-46

Parts with the exploded numbers larger than 700 are not supplied.

X29-1610-00
IC1 : TC40H004P
IC2 : UPD4011BC or TC4011BP
IC3 : CX-20109
IC4 : AN6555
Q1,3 : 2SC1815(Y,GR), 2SC945(A)(Q,P) or 2SC2320(E,F)
Q2 : 2SA1015(Y,GR), 2SA733(A)(Q,P) or 2SA999(E,F)
Q4 : 2SD571
Q5 : 2SB514
Q6 : 2SK301
D1,4,5 : 1SS176 or GMA01
D2,3 : RD4.7E(B2)

X32-1020-00
IC1 : TD6315AP
IC2 : TC9178F
IC3 : HM6116FP-4 or MB8418-20LPF
IC4 : TC9179F
Q1 : 2SA1015(Y,GR), 2SA733(A)(Q,P) or 2SA1127NC(R,S)
Q2,3 : 2SC1815(Y,GR), 2SC945(A)(Q,P) or 2SC1685(R,S)
Q4 : 2SC1923(Y)
D1 : RD8.2E(B2)
D2~5 : 1SS176 or GMA01
D6 : 1SV147

X29-1600-11
IC1,4 : AN6555
IC2,3 : TA7256P
IC7 : TRD5010
IC5,8 : TA75393S or AN6913
IC6 : μPA80C
IC10 : μPD7519G-151-36
IC9 : TC40H000P
IC11 : CX20017
IC13 : TL084CN
IC14 : NJM4560D-N
IC17 : μPC4557C
IC12 : μPD4053BC
IC15 : μPC78L12
IC16 : NJM79L12A

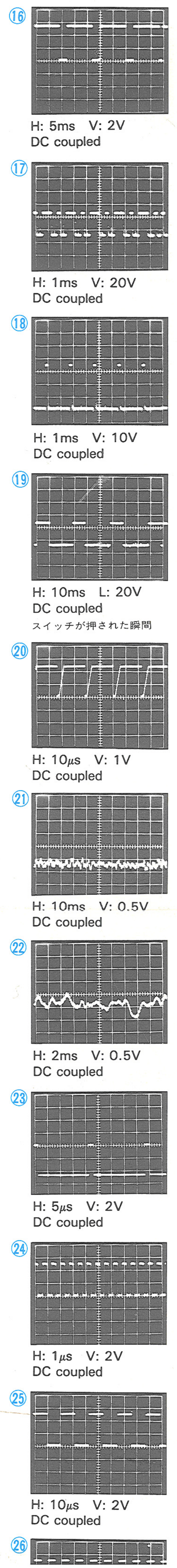

CONTROL (X29-1600-11) (A/6)
X29 (D/6)
TRACKING SERVO
X29 (C/6)
FEED MOTOR DR
TRAKING DR
FOCUS SERVO AMP
TEST PIN
TRACKING GAIN ADJUST
BRAKE
MEMORY
ERROR CORRECTION
FUNCTION/SEARCH
DISC MOTOR DR
DROPOUT CONT
TRAY MOTOR DR
RF DETECT
BRAKE
EMPHASIS
ANALOG CIRCUIT
SAMPLING
LPF
FWOB
20 FEED MOTOR
13 S.GND
12 D-CON
11 +5V
8 S.GND
4 RF
R.CH
L.CH
OUT PUT
X29 F/6
(U,M,X,T,E)
120V~/220-240V 50/60Hz

CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list).

⚠ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

DESTINATION	K,P,U,M,X,T	E
X29-160	0-11	2-71
C132 ~ 134	NO	YES
C137,138	NO	YES

Q1,2,6,7,9 : 2SK301
Q3~5,8,10,11,38~41 : 2SC2878
Q12,14,18,25,29 : 2SC1815(Y,GR),
2SC945(A)(Q,P)or


⑯ H: 5ms V: 2V
DC coupled

⑰ H: 1ms V: 20V
DC coupled

⑱ H: 1ms V: 10V
DC coupled

⑲ H: 10ms L: 20V
DC coupled
スイッチが押された瞬間

⑳ H: 10μs V: 1V
DC coupled

㉑ H: 10ms V: 0.5V
DC coupled

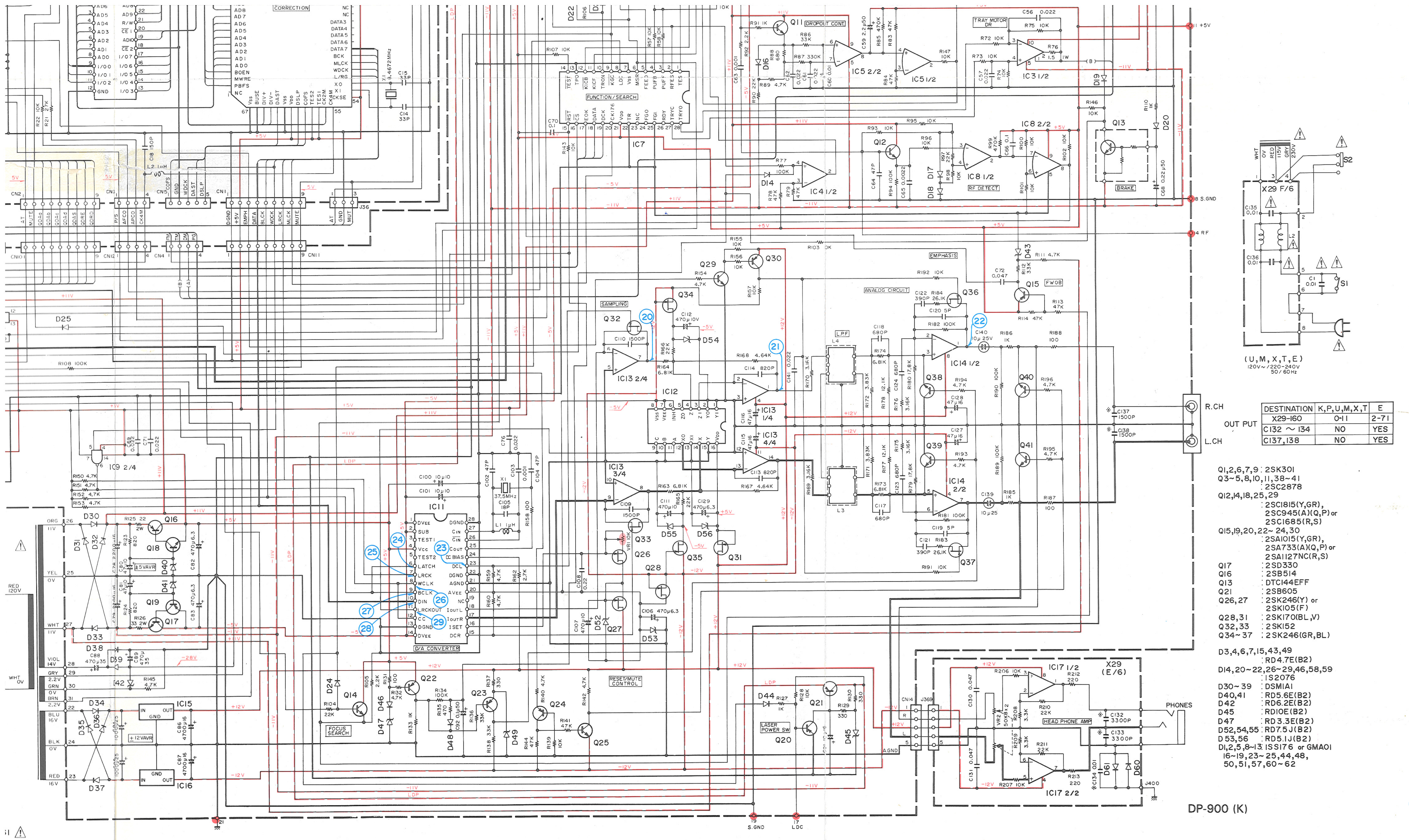
㉒ H: 2ms V: 0.5V
DC coupled

㉓ H: 5μs V: 2V
DC coupled

㉔ H: 1μs V: 2V
DC coupled

㉕ H: 10μs V: 2V
DC coupled

㉖

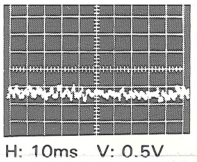

CORRECTION
FUNCTION/SEARCH
IC7
DROPOUT CONT
TRAY MOTOR DR
IC5 2/2
IC5 1/2
IC3 1/2
IC8 2/2
IC8 1/2
RF DETECT
IC4 1/2
BRAKE
EMPHASIS
FWOB
ANALOG CIRCUIT
SAMPLING
LPF
IC14 1/2
IC14 2/2
IC13 2/4
IC13 1/4
IC13 4/4
IC13 3/4
IC12
IC11
D/A CONVERTER
IC9 2/4
IC15
IC16
FOCUS SEARCH
RESET/MUTE CONTROL
LASER POWER SW
HEAD PHONE AMP
IC17 1/2
IC17 2/2
X29 (E/6)
X29 F/6
PHONES
R.CH
L.CH
OUT PUT
S.GND
LDP
+5V
RF
(U,M,X,T,E)
120V~/220-240V
50/60Hz

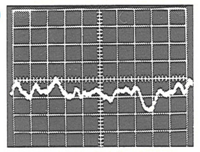
DESTINATION	K,P,U,M,X,T	E
X29-160	0-11	2-71
C132 ~ 134	NO	YES
C137,138	NO	YES

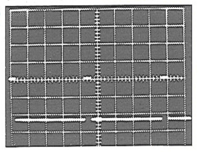
Q1,2,6,7,9 : 2SK301
Q3~5,8,10,11,38~41
: 2SC2878
Q12,14,18,25,29
: 2SC1815(Y,GR),
2SC945(A)(Q,P) or
2SC1685(R,S)
Q15,19,20,22~24,30
: 2SA1015(Y,GR),
2SA733(A)(Q,P) or
2SA1127NC(R,S)
Q17 : 2SD330
Q16 : 2SB514
Q13 : DTC144EFF
Q21 : 2SB605
Q26,27 : 2SK246(Y) or
2SK105(F)
Q28,31 : 2SK170(BL,V)
Q32,33 : 2SK152
Q34~37 : 2SK246(GR,BL)

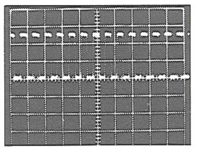
D3,4,6,7,15,43,49
: RD4.7E(B2)
D14,20~22,26~29,46,58,59
: 1S2076
D30~39 : DSM1A1
D40,41 : RD5.6E(B2)
D42 : RD6.2E(B2)
D45 : RD10E(B2)
D47 : RD3.3E(B2)
D52,54,55 : RD7.5J(B2)
D53,56 : RD5.1J(B2)
D1,2,5,8~13 : 1SS176 or GMA01
16~19,23~25,44,48,
50,51,57,60~62

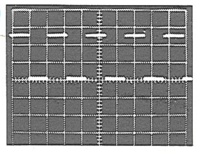
DP-900 (K)

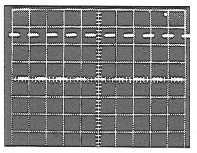
㉑

H: 10ms V: 0.5V
DC coupled

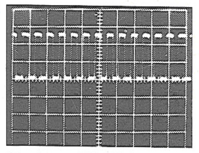
㉒

H: 2ms V: 0.5V
DC coupled

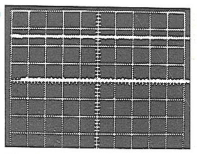
㉓

H: 5µs V: 2V
DC coupled

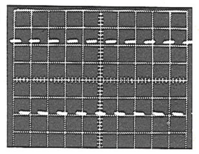
㉔

H: 1µs V: 2V
DC coupled

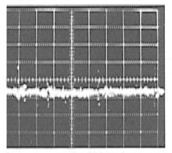
㉕

H: 10µs V: 2V
DC coupled

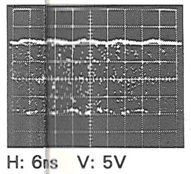
㉖

H: 10µs V: 2V
DC coupled

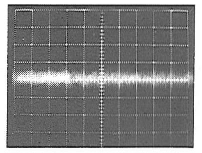
㉗

H: 1µs V: 2V
DC coupled

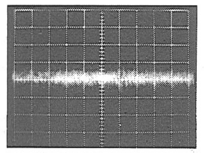
㉘

H: 1µs V: 2V
DC coupled

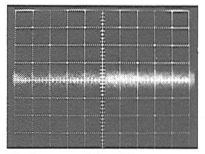
㉙

H: 20µs V: 2V
DC coupled

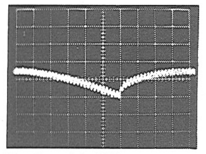

6ms V: 2V
coupled

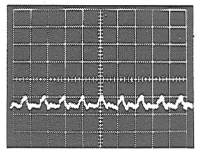
⑦

H: 6ms V: 5V
DC coupled

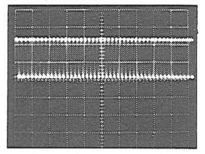
⑧

H: 6ms V: 100mV
DC coupled

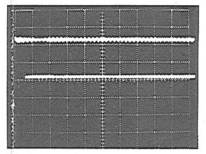
⑨

H: 6ms V: 0.5V
DC coupled

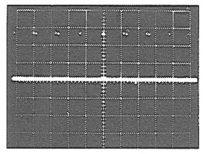
⑩

H: 6ms V: 2V
DC coupled

⑪

H: 1s V: 1V
DC coupled
オシロMEMORY波形

⑫

H: 50ms V: 1V
DC coupled
オシロMEMORY波形

⑬

H: 1µs V: 2V
DC coupled

⑭

H: 1µs V: 2V
DC coupled

⑮

H: 10ms V: 2V
DC coupled

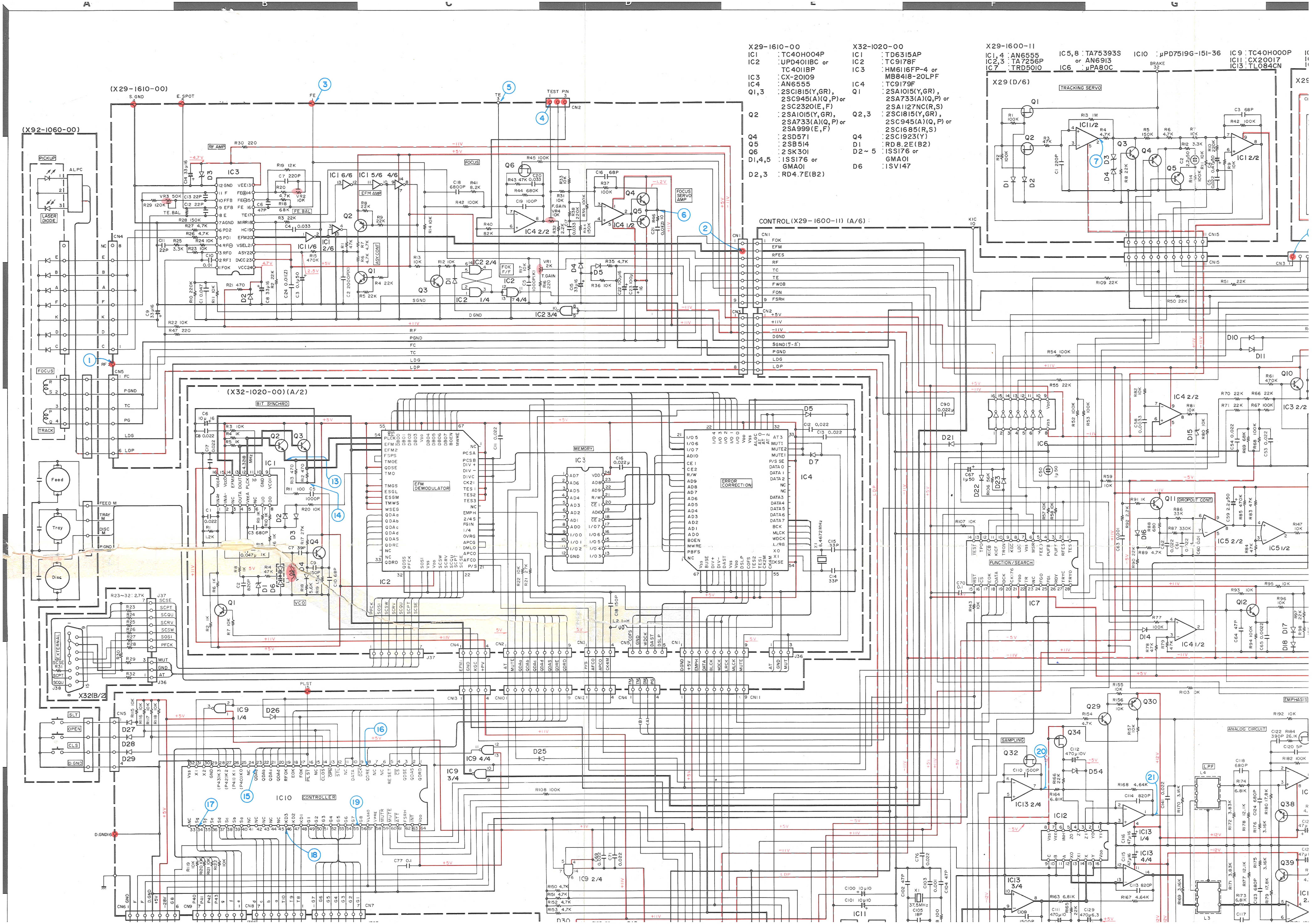
DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Les tensions c.c. doivent être mesurées avec un voltmètre à haute impédance. Les valeurs peuvent différer légèrement du fait des variations inhérentes aux appareils et aux instruments de mesure individuels.

Die angegebenen Gleichspannungswerte wurden mit einem hochohmigen Spannungsmesser gemessen. Dabei schwanken die Meßwerte aufgrund von Unterschieden zwischen einzelnen Instrumenten oder Geräten u.U. geringfügig.

DP-900

KENWOOD



A
B
C
D
E
F
G
(X92-1060-00)
PICKUP
ALPC
LASER DIODE
FOCUS
TRACK
Feed
Tray
Disc
(X29-1610-00)
S.GND
E.SPOT
FE
TE
TEST PIN
CN2
RF AMP
IC3
FOCUS
EFM AMP
FE BAL
TE.BAL
ASY CONT
F.GAIN
T.GAIN
FOCUS SERVO AMP
IC4 2/2
IC4 1/2
IC1 6/6
IC1 5/6
IC1 4/6
IC1 1/6
IC1 2/6
IC2 2/4
IC2 1/4
IC2 3/4
IC2 4/4
FOK F/F
SGND
D GND
CONTROL (X29-1600-11) (A/6)
CN1
FOK
EFM
RFES
RF
TC
TE
FWOB
FON
FSRH
CN2
+5V
+11V
-11V
DGND
SGND(サーボ)
PGND
LDG
LDP
RF
PGND
FC
TC
LDG
LDP
(X32-1020-00)(A/2)
BIT SYNCHRO
IC1
VCO
EFM DEMODULATOR
IC2
MEMORY
IC3
ERROR CORRECTION
IC4
X1 8.4672MHz
J37
J36
J38
EXTERNAL
X32(B/2)
R23~32: 2.7K
SCSE
SCPT
SCQU
SCRV
SCSW
SOSI
PFCK
MUT
GND
AT
PLST
SLT
OPEN
CLS
D.GND
D.GND
IC9 1/4
IC9 4/4
IC9 3/4
IC9 2/4
IC10
CONTROLLER
IC11
X1 37.5MHz
X29(D/6)
TRACKING SERVO
BRAKE 32
IC1 1/2
IC1 2/2
IC4 2/2
IC3 2/2
IC6
FUNCTION/SEARCH
IC7
IC5 2/2
IC5 1/2
IC4 1/2
DROPOUT CONT
SAMPLING
IC12
IC13 2/4
IC13 1/4
IC13 4/4
IC13 3/4
EMPHASIS
ANALOG CIRCUIT
LPF
①
②
③
④
⑤
⑥
⑦
⑬
⑭
⑮
⑯
⑰
⑱
⑲
⑳
㉑

X29-1610-00

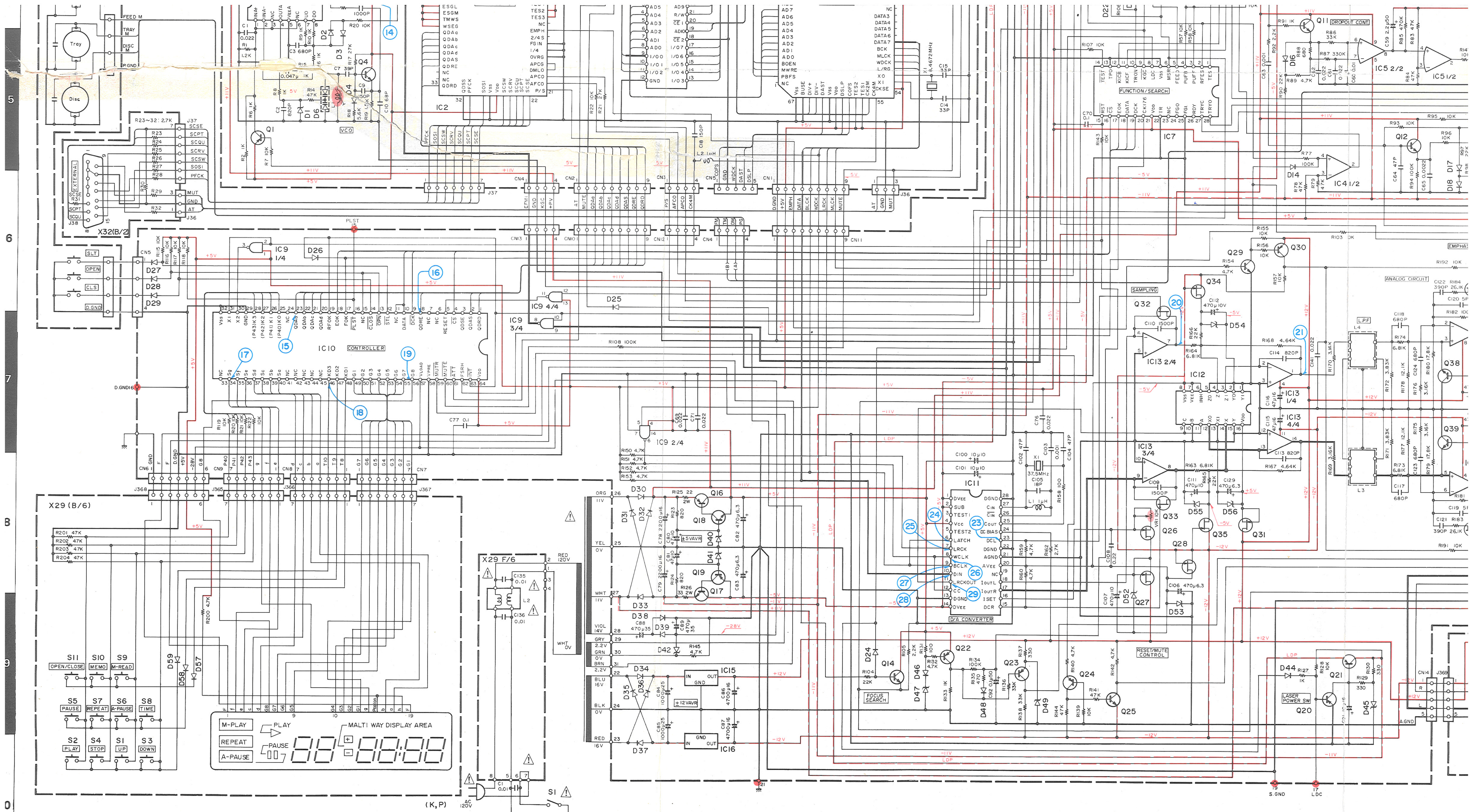
IC1	: TC40H004P
IC2	: UPD4011BC or TC4011BP
IC3	: CX-20109
IC4	: AN6555
Q1,3	: 2SC1815(Y,GR), 2SC945(A)(Q,P) or 2SC2320(E,F)
Q2	: 2SA1015(Y,GR), 2SA733(A)(Q,P) or 2SA999(E,F)
Q4	: 2SD571
Q5	: 2SB514
Q6	: 2SK301
D1,4,5	: 1SS176 or GMA01
D2,3	: RD4.7E(B2)

X32-1020-00

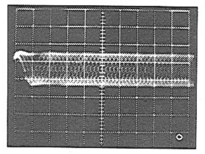
IC1	: TD6315AP
IC2	: TC9178F
IC3	: HM6116FP-4 or MB8418-20LPF
IC4	: TC9179F
Q1	: 2SA1015(Y,GR), 2SA733(A)(Q,P) or 2SA1127NC(R,S)
Q2,3	: 2SC1815(Y,GR), 2SC945(A)(Q,P) or 2SC1685(R,S)
Q4	: 2SC1923(Y)
D1	: RD8.2E(B2)
D2~5	: 1SS176 or GMA01
D6	: 1SV147

X29-1600-11

IC1,4	: AN6555
IC2,3	: TA7256P
IC7	: TRD5010
IC5,8	: TA75393S or AN6913
IC6	: μPA80C
IC10	: μPD7519G-151-36
IC9	: TC40H000P
IC11	: CX20017
IC13	: TL084CN

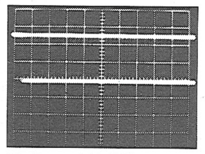

FEED M
TRAY M
DISC M
Tray
Disc
P.GND
J37
SCSE
SCPT
SCQU
SCRV
SCSW
SOSI
PFCK
MUT
GND
AT
J36
J38
EXTERNAL
X32(B/2)
R23~32: 2.7K
Q1
Q4
VCO
IC2
IC7
FUNCTION/SEARCH
DROPOUT CONT
IC5 2/2
IC5 1/2
IC4 1/2
Q11
Q12
8.4672MHz
CN4
CN2
CN3
CN5
CN1
J36
CN13
CN10
CN12
CN4
CN11
PLST
IC9 1/4
D26
D25
IC9 4/4
IC9 3/4
IC10
CONTROLLER
SLT
OPEN
CLS
D.GND
CN5
D27
D28
D29
D.GND
IC9 2/4
CN6
CN9
CN8
CN7
J368
J365
J366
J367
X29 (B/6)
R201 47K
R202 47K
R203 47K
R204 47K
S11 OPEN/CLOSE
S10 MEMO
S9 M-READ
S5 PAUSE
S7 REPEAT
S6 A-PAUSE
S8 TIME
S2 PLAY
S4 STOP
S1 UP
S3 DOWN
M-PLAY
REPEAT
A-PAUSE
PLAY
PAUSE
MALTI WAY DISPLAY AREA
X29 F/6
RED 120V
WHT 0V
AC 120V
S1
(K,P)
ORG 11V
YEL 0V
WHT 11V
VIOL 14V
GRY 2.2V
GRN 0V
BRN 2.2V
BLU 16V
BLK 0V
RED 16V
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
D42
Q16
Q17
Q18
Q19
+5VAVR
+12VAVR
IC15
IC16
IC11
D/A CONVERTER
37.5MHz
SAMPLING
Q32
IC13 2/4
IC12
IC13 3/4
Q33
Q34
Q26
Q28
Q35
Q31
Q27
D52
D53
D54
D55
D56
Q29
Q30
EMPHASIS
ANALOG CIRCUIT
LPF
L4
L3
IC13 1/4
IC13 4/4
Q38
Q39
D24
Q14
FOCUS SEARCH
D46
D47
Q22
Q23
D48
D49
Q24
Q25
RESET/MUTE CONTROL
D44
Q21
LASER POWER SW
Q20
D45
CN14
J369
AGND
S.GND
LDC
14
15
16
17
18
19
20
21
23
24
25
26
27
28
29

①



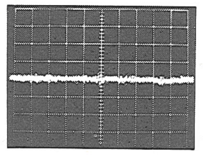
H: 1μs V: 1V
AC coupled

②



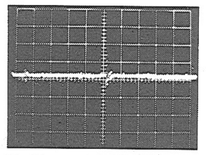
H: 1μs V: 1V
AC coupled

③



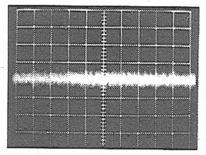
H: 10ms V: 0.5V
DC coupled

④



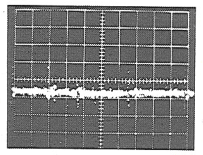
H: 5ms V: 0.5V
DC coupled

⑤



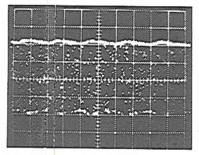
H: 5ms V: 0.5V
DC coupled

⑥



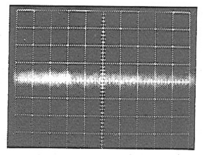
H: 6ms V: 2V
DC coupled

⑦



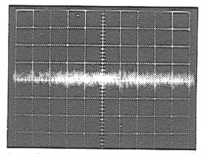
H: 6ms V: 5V
DC coupled

⑧



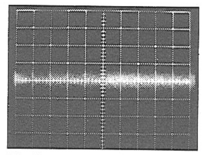
H: 6ms V: 100mV
DC coupled

⑨



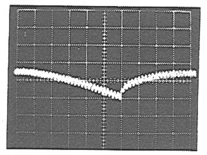
H: 6ms V: 0.5V
DC coupled

⑩



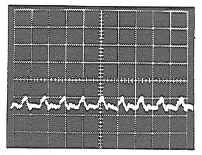
H: 6ms V: 2V
DC coupled

⑪



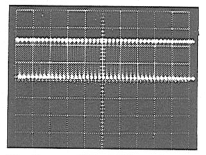
H: 1s V: 1V
DC coupled
オシロMEMORY波形

⑫



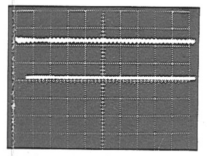
H: 50ms V: 1V
DC coupled
オシロMEMORY波形

⑬



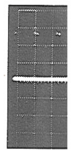
H: 1μs V: 2V
DC coupled

⑭



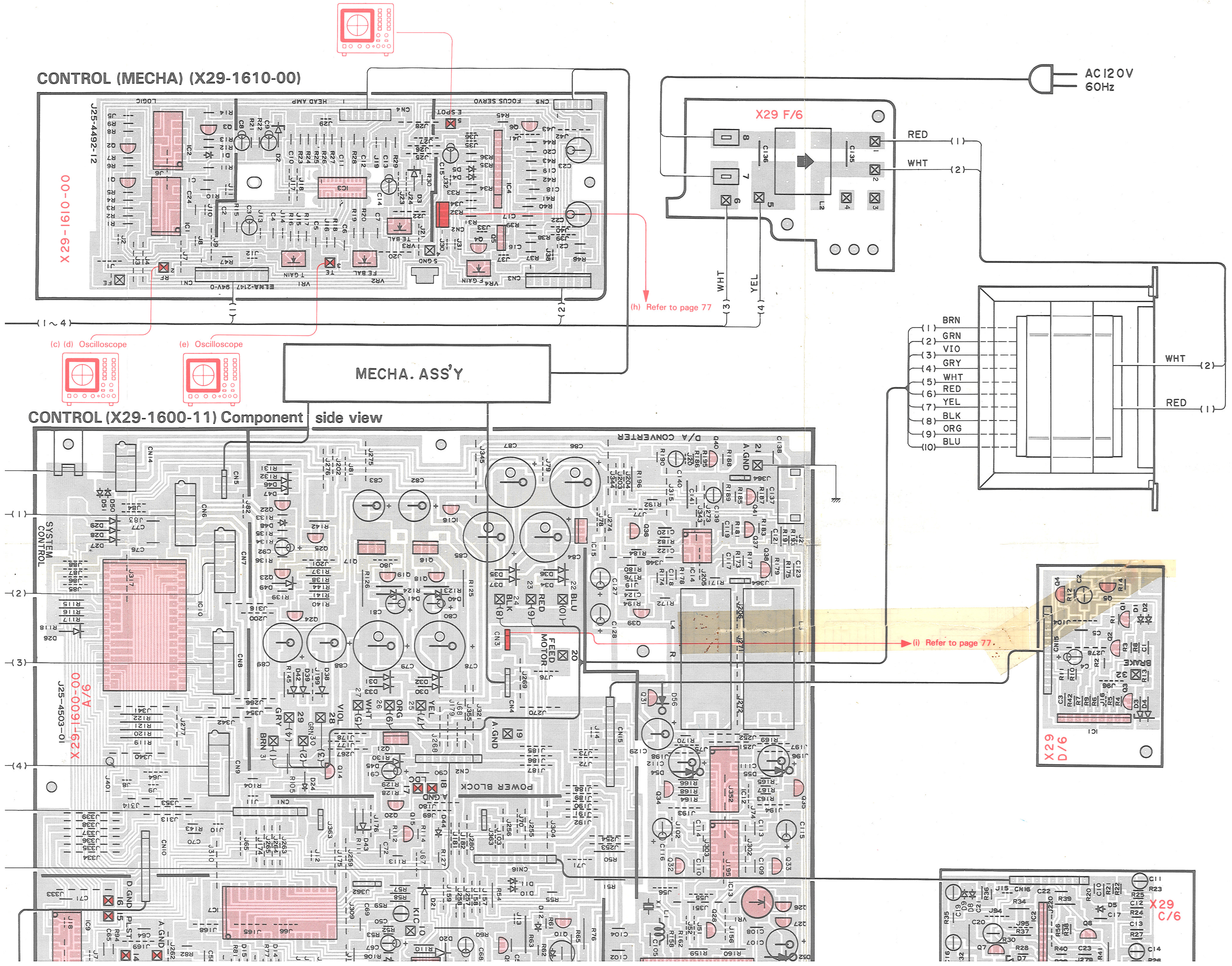
H: 1μs V: 2V
DC coupled

⑮



H: 10m
DC cou

9. PC BOARD



(f) Oscilloscope
CONTROL (MECHA) (X29-1610-00)
X29-1610-00
J25-4492-12
AC120V
60Hz
X29 F/6
RED
WHT
WHT
YEL
(h) Refer to page 77
(c) (d) Oscilloscope
(e) Oscilloscope
MECHA. ASS'Y
CONTROL (X29-1600-11) Component side view
BRN
GRN
VIO
GRY
WHT
RED
YEL
BLK
ORG
BLU
WHT
RED
D/A CONVERTER
SYSTEM CONTROL
FEED MOTOR
POWER BLOCK
X29-1600-00 A/6
J25-4503-01
(i) Refer to page 77.
X29 D/6
BRAKE
X29 C/6

○number (Blue); Refer to schematic diagram on the reverse side.

X29-1610-00

Q2

E	5V
C	–
B	–

Q4

E	⑥
C	11V
B	–

Q5

E	⑥
C	–11V
B	–

IC1

2	②
3	
5	0V
7	
14	5V

IC2

7	0V
14	5V

IC3

2	1
7	0V
12	
13	–4.7V
16	③
21	5V
22	2.5V
23	5V
24	4.7V

IC4

1	11V
4	0V
5	–11V

Terminal

RF (2)	①
FE (1)	③
TE (3)	⑤
CN2 (1)	④
CN1 (2)	②

X29-1600-00

Q1

E	⑧
C	0 V
B	–

Q7

G	–
D	–
S	⑩

Q9

G	–
D	–
S	12

Q10

E	–
C	11V
B	–

Q11

E	–
C	11V
B	–

Q12

E	–
C	11V
B	–

Q13

E	–11V
C	–
B	–

Q14

E	–
C	5V
B	–

Q15

E	5V
C	–
B	–

Q16

E	–
C	5V
B	–

Q17

E	–
C	–5V
B	–

Q18

E	5V
C	–
B	–

Q19

E	–5V
C	–
B	–

Q21

E	–
C	–11V
B	–

Q27

G	–
D	12V
B	–

Q28

G	–12V
D	–
S	–2V

Q30

E	12V
C	–
B	–

Q31

G	5V
D	12V
S	5V

Q34

G	–12V
D	–
S	–12V

Q35

G	–12V
D	–
S	–12V

Q36

G	–
D	㉒
S	–

IC1

2	⑦
3	0V
5	–11V
8	⑨
9	11V

IC2

5	–11V
10	11V

X32-1020-00

Q1

E	5V
C	–
B	–

Q2

E	⑬
C	5V
B	–

Q3

E	⑭
C	5V
B	–

Q4

E	–
C	5V
B	–

IC1

5	0V
10	
15	5V
16	11V

IC2

2	5V

X29-1600-00

IC3

5	–11V
6	0 V
10	11C

IC4

5	–11V
9	11V

IC5

5	–1V
9	11V

IC6

8	–11V
9	5V

IC7

7	0V
13	
21	5V
25	0V

IC8

5	0V
9	0V

IC10

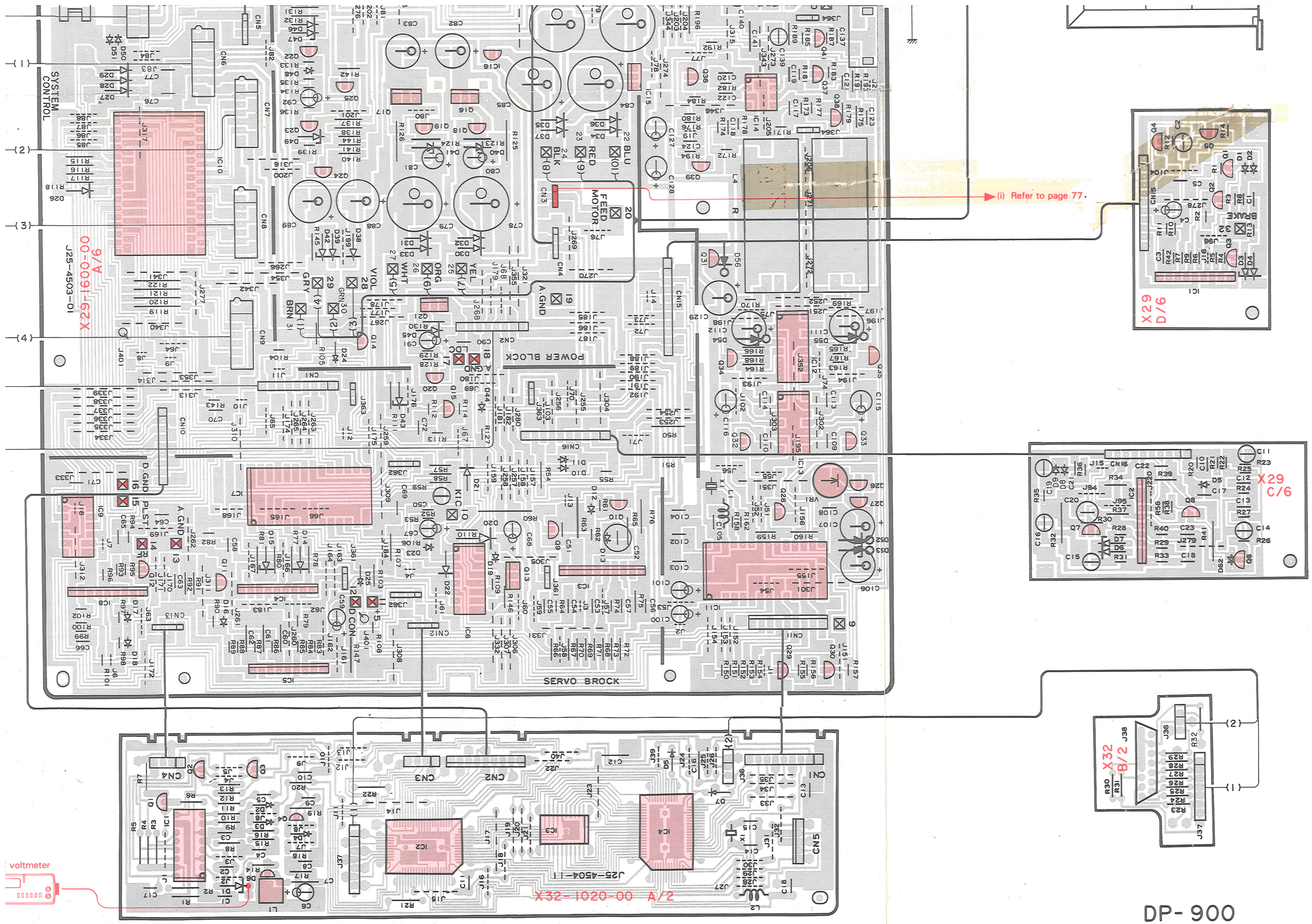
8	⑯
23	⑮
29	0V
32	
34	⑰
46	⑱
56	⑲
58	0V
64	5V

IC12

1	–5V
2	
5	
6	–5V
7	
8	
9	㉙
10	0V
11	㉙
13	0V
15	
16	5V

IC13

1	⑫


SYSTEM CONTROL
(1)
(2)
(3)
(4)
X29-1600-00 A/6
J25-4503-01
POWER BLOCK
SERVO BROCK
FEED MOTOR
A GND
D GND
PLST
RED
BLK
BLU
GRY
BRN
ORG
WHT
VIOL
YEL
GRN
X29 D/6
X29 C/6
X32 B/2
X32-1020-00 A/2
J25-4504-11
voltmeter

(i) Refer to page 77.

PROCESSOR (X32-1020-00) Component side view

4	0V
5	−11V

Terminal

RF (2)	①
FE (1)	③
TE (3)	⑤
CN2 (1)	④
CN1 (2)	②

Q15

E	5V
C	−
B	−

Q16

E	−
C	5V
B	−

Q17

E	−
C	−5V
B	−

G	−
D	㉒
S	−

IC1

2	⑦
3	0V
5	−11V
8	⑨
9	11V

IC2

5	−11V
10	11V

X32-1020-00

Q1

E	5V
C	−
B	−

Q2

E	⑬
C	5V
B	−

Q3

E	⑭
C	5V
B	−

Q4

E	−
C	5V
B	−

IC1

5	0V
10	
15	5V
16	11V

IC2

2	5V	36	⑯
3	0V	41	⑮
6		42	5V
21	5V	46	
27		49	
28	0V	53	14
32		54	⑬
		61	5V

IC3

12	0V
18	
24	5V

IC4

27	5V
28	0V
29	
37	5V
47	㉘
48	㉔, ㉗
51	㉕
54	5V
55	
57	5V
58	
61	
62	0V
66	0V
67	

X29-1600-00

IC3

5	−11V
6	0 V
10	11C

IC4

5	−11V
9	11V

IC5

5	−1V
9	11V

IC6

8	−11V
9	5V

IC7

7	0V
13	
21	5V
25	0V

IC8

5	0V
9	0V

IC10

8	⑯
23	⑮
29	0V
32	
34	⑰
46	⑱
56	⑲
58	0V
64	5V

IC12

1	−5V
2	
5	
6	−5V
7	
8	
9	㉙
10	0V
11	㉙
13	0V
15	
16	5V

IC13

1	⑫
3	0V
4	12V
5	0V
7	⑳
10	0V
11	−12V
12	0V

IC14

1	㉒
4	−12V
8	12V

IC11

1	−5V	11	㉙
2		12	㉖
4	5V	13	0V
6	24	14	−5V
7	㉕	21	0V
8	㉖	23	㉓
9	㉗	28	0V
10	㉘		

IC15

IN	−
GND	0V
OUT	12V

IC16

IN	−
GND	0V
OUT	12V

IC17

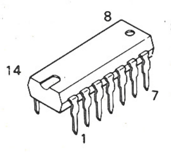
4	−12V
B	12V

Terminal

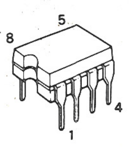
CN3 (1)	⑧
CN6 (1)	⑨
CN6 (8)	⑩
F.M (20)	⑪

DP-900

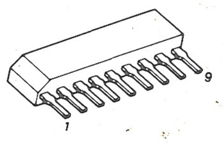
TL084CN



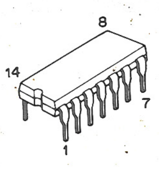
UPC4557C



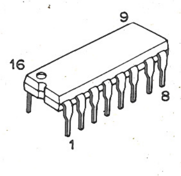
AN6555
AN6913



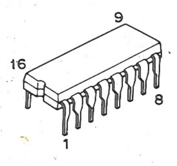
TC40H000P
TC40H004P
TC4011BP
UPD4011BC



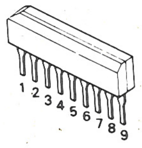
TD6315AP



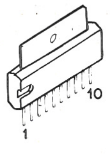
UPA80C
UPD4053BC



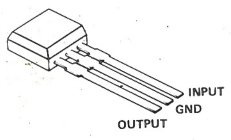
TA75393S



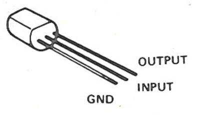
TA7256P



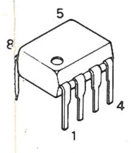
UPC78L12


INPUT
GND
OUTPUT

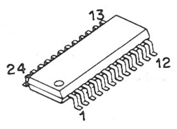
NJM79L12A


OUTPUT
INPUT
GND

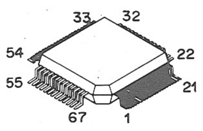
NJM4560D-N



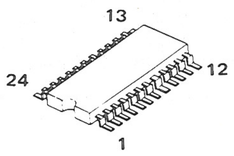
CX-20109
MB8418-20LPF



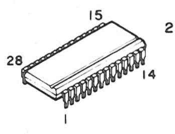
TC9178AF
TC9179F


33
32
54
22
55
21
67
1

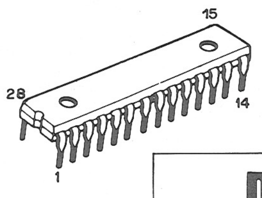
HM6116FP-4



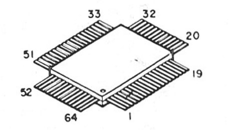
TRD5010



CX-20017



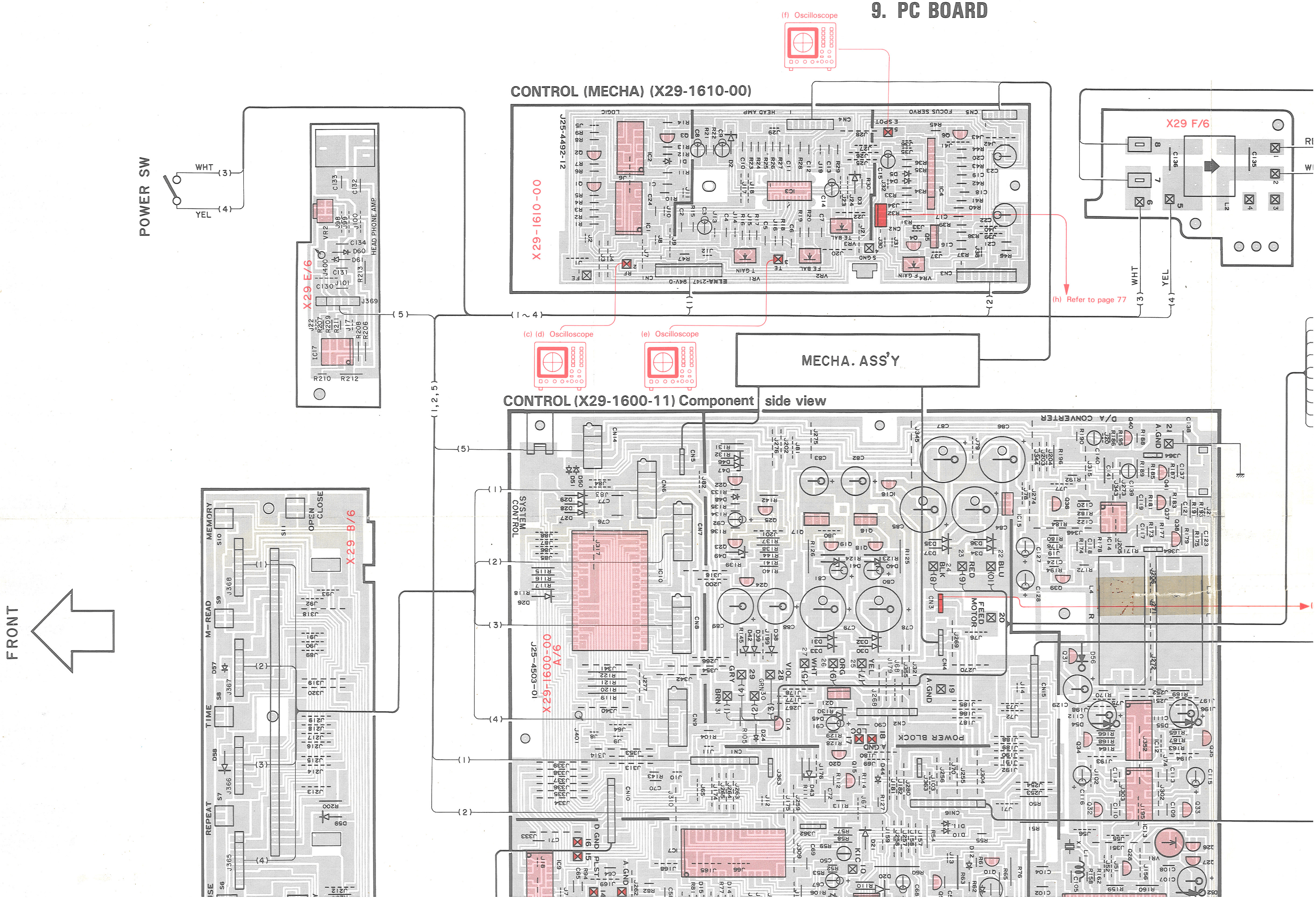
UPD7519G-167-36

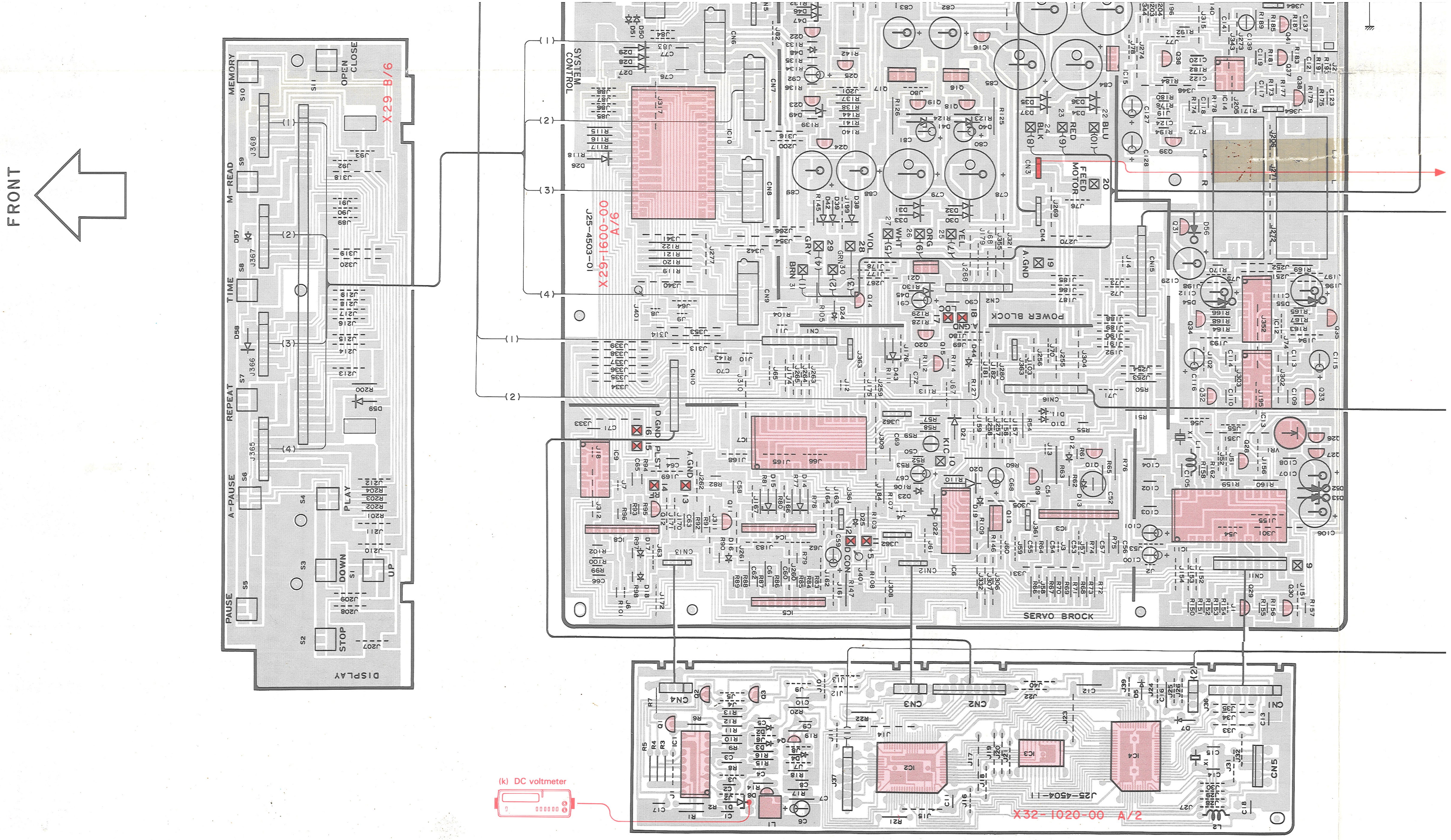

33
32
51
20
52
19
64
1

Refer to the schematic diagram for the values of resistors and capacitors.
The PC board drawing is viewing from the side easy to check.

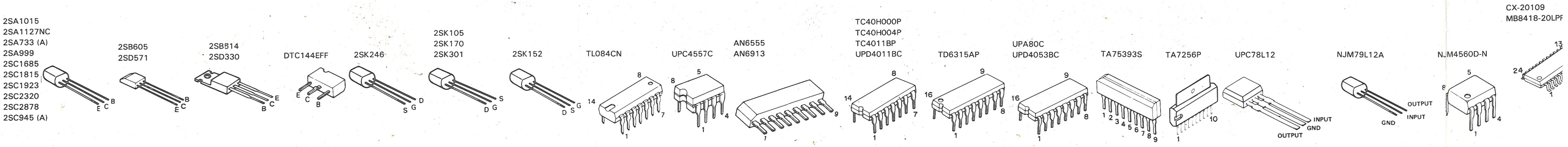
DP-900
KENWOOD

9. PC BOARD


(f) Oscilloscope
CONTROL (MECHA) (X29-1610-00)
X29-1610-00
J25-4492-12
X29 F/6
(h) Refer to page 77
WHT
YEL
POWER SW
WHT
YEL
X29 E/6
HEAD PHONE AMP
(c) (d) Oscilloscope
(e) Oscilloscope
MECHA. ASS'Y
CONTROL (X29-1600-11) Component side view
D/A CONVERTER
SYSTEM CONTROL
X29-1600-00 A/6
J25-4503-01
FEED MOTOR
POWER BLOCK
A.GND
D.GND
X29 B/6
MEMORY
OPEN CLOSE
M-READ
TIME
REPEAT
FRONT
(1~4)
(5)
(1,2,5)
(1)
(2)
(3)
(4)


FRONT
DISPLAY
MEMORY
OPEN CLOSE
M-READ
TIME
REPEAT
A-PAUSE
PAUSE
STOP
DOWN
UP
PLAY
X29 B/6
SYSTEM CONTROL
J25-4503-01
X29-1600-00 A/6
FEED MOTOR
POWER BLOCK
SERVO BROCK
A.GND
D.GND
(k) DC voltmeter
J25-4504-11
X32-1020-00 A/2
CN1
CN2
CN3
CN4
CN5
IC1
IC2
IC3
IC4

PROCESSOR (X32-1020-00) Component side view


2SA1015
2SA1127NC
2SA733 (A)
2SA999
2SC1685
2SC1815
2SC1923
2SC2320
2SC2878
2SC945 (A)
E C B
2SB605
2SD571
E C B
2SB514
2SD330
B C E
DTC144EFF
E C B
2SK246
S G D
2SK105
2SK170
2SK301
D G S
2SK152
D S G
TL084CN
14 8 1 7
UPC4557C
8 5 1 4
AN6555
AN6913
1 9
TC40H000P
TC40H004P
TC4011BP
UPD4011BC
14 8 1 7
TD6315AP
16 9 1 8
UPA80C
UPD4053BC
16 9 1 8
TA75393S
1 2 3 4 5 6 7 8 9
TA7256P
1 10
UPC78L12
INPUT
GND
OUTPUT
NJM79L12A
OUTPUT
INPUT
GND
NJM4560D-N
8 5 1 4
CX-20109
MB8418-20LPF
24 13 1

10. PARTS LIST

⁎ New Parts
Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
				DP-900		
201	1C	*	A01-1379-02	METALLIC CABINET		
202	3C	*	A20-4156-03	PANEL ASSY	KPUMX	
202	3C	*	A20-4156-03	PANEL ASSY	E	
202	3C	*	A20-4213-03	PANEL ASSY	T	
203	2C	*	A29-0051-03	PANEL (TRAY)		
207	3D		B10-0566-14	FRONT GLASS		
-			B46-0092-03	WARRANTY CARD	K	
-			B46-0094-03	WARRANTY CARD	U	
-			B46-0095-03	WARRANTY CARD	U	
-			B46-0096-03	WARRANTY CARD	X	
-			B46-0121-03	WARRANTY CARD	P	
-			B46-0122-03	WARRANTY CARD	E	
-			B46-0123-03	WARRANTY CARD	T	
-		*	B50-5566-00	INSTRUCTION MANUAL(ENGLISH)	KPUMX	
-		*	B50-5566-00	INSTRUCTION MANUAL(ENGLISH)	E	
-		*	B50-5567-00	INSTRUCTION MANUAL(FRENCH)	PMXE	
-		*	B50-5568-00	INSTRUCTION MANUAL(SPANISH)	M	
-		*	B50-5569-00	INSTRUCTION MANUAL(ENGLISH)	T	
-		*	B50-5570-00	INSTRUCTION MANUAL(G,D,I)	E	
-			B58-0223-04	CAUTION CARD (PRESET 120V)	U	
-			B58-0269-04	CAUTION CARD	K	
-		*	B58-0326-04	CAUTION CARD		
-		*	B58-0327-04	CAUTION CARD		
-			B59-0092-00	SERVICE DIRECTORY	U	
⚠ C1	2D		C91-0023-05	CERAMIC 0.01UF AC250V	UM	
⚠ C1	2D		C91-0647-05	CERAMIC 0.01UF P	KPXTE	
211	1D		E30-0505-05	AUDIO CORD		
⚠ 212	1F		E30-0181-05	AC POWER CORD	K	
⚠ 212	1F		E30-0459-05	AC POWER CORD	E	
⚠ 212	1F		E30-0587-15	AC POWER CORD	T	
⚠ 212	1F		E30-0780-05	AC POWER CORD	P	
⚠ 212	1F		E30-0812-05	AC POWER CORD	UM	
⚠ 212	1F		E30-1341-05	AC POWER CORD	X	
-		*	H01-5360-04	ITEM CARTON CASE	T	
-		*	H01-5362-04	ITEM CARTON CASE	KPUMX	
-		*	H01-5362-04	ITEM CARTON CASE	E	
-		*	H10-1779-02	POLYSTYRENE FOAMED FIXTURE		
-		*	H12-0186-04	PACKING FIXTURE		
-			H20-0417-04	PROTECTION COVER(460X370X360)	M	
-			H25-0078-04	PROTECTION BAG (235X315)		
-			H25-0224-04	PROTECTION BAG (800X400)	KPUXT	
-			H25-0224-04	PROTECTION BAG (800X400)	E	
-			H40-0005-04	RUST PREVENTING PAPER(380X250)	M	
216	3E,3F		J02-0126-05	FOOT		
⚠ 217	1F		J42-0083-05	POWER CORD BUSHING		
218	2B	*	J91-0246-05	PICKUP		
-			J61-0307-05	WIRE BAND		
221	2C		K27-1082-04	KNOB (BUTTON) POWER		
222	3C		K29-1964-04	KNOB PHONES LEVEL		
223	2D	*	K29-1945-03	KNOB ASSY(BTN) OPERATION SW		
⚠ 227	1E	*	L01-3851-05	POWER TRANSFORMER	KP	

E: Scandinavia & Europe H:Audio Club K: USA P: Canada
S: South Africa T: England U: PX(Far East, Hawaii)
UE: AAFES(Europe) X: Australia M: Other Areas

⚠ indicates safety critical components.

10. PARTS LIST

⁎ New Parts

Parts without **Parts No.** are not supplied.

Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.

Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
⚠ 227	1E	⁎	L01-3854-05	POWER TRANSFORMER	UMXTE	
A	2C	⁎	N09-1445-05	SET SCREW (M3X8) PANEL		
B	2D,2E		N29-0035-05	PUSH RIVET (Ø3.5X5.5)		
D	2A,1E		N09-0976-05	TAPTITE SCREW(M3X6)		
⚠ S1	2D		S40-1067-05	PUSH SWITCH (POWER TYPE)		
⚠ S2	2D		S31-2083-05	SLIDE SWITCH (POWER TYPE)	UMXTE	

CONTROL CIRCUIT (X29-1600-11)

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti-nation 仕向	Re-marks 備考
C1			CC45FSL1H221J	CERAMIC 220PF J		
C2			CE04HW1H2R2M	NP-ELEC 2.2UF 50WV		
C3			CC45FSL1H680J	CERAMIC 68PF J		
C4			CE04FW1HR47M	ELECTRO 0.47UF 50WV		
C5			CF92FV1H223J	MF 0.022UF J		
C10			CF92FV1H104J	MF 0.10UF J		
C11			CE04HW1E4R7M	NP-ELEC 4.7UF 25WV		
C12			CF92FV1H682J	MF 6800PF J		
C13			CF92FV1H472J	MF 4700PF J		
C14			CE04HW1HR33M	NP-ELEC 0.33UF 50WV		
C15			CE04HW1E220M	NP-ELEC 22UF 25WV		
C16			CE04HW1E100M	NP-ELEC 10UF 25WV		
C17			CC45FSL1H470J	CERAMIC 47PF J		
C18			CK45FF1H223Z	CERAMIC 0.022UF Z		
C19			CE04HW1E4R7M	NP-ELEC 4.7UF 25WV		
C20			CE04HW1E220M	NP-ELEC 22UF 25WV		
C21			CK45FF1H473Z	CERAMIC 0.047UF Z		
C22			CC45FSL1H221J	CERAMIC 220PF J		
C23			CK45FF1H223Z	CERAMIC 0.022UF Z		
C50			CE04HW1H010M	NP-ELEC 1.0UF 50WV		
C51			CF92FV1H392J	MF 3900PF J		
C52			CE04HW1H3R3M	NP-ELEC 3.3UF 50WV		
C53 -57			CK45FF1H223Z	CERAMIC 0.022UF Z		
C58			CK45FB1H332K	CERAMIC 3300PF K		
C59			CE04FW1H2R2M	ELECTRO 2.2UF 50WV		
C60			C91-0083-05	CERAMIC 0.01UF N		
C61 ,62			C91-0085-05	CERAMIC 0.022UF N		
C63			CK45FB1H102K	CERAMIC 1000PF K		
C64			CC45FSL1H470J	CERAMIC 47PF J		
C65			CK45FB1H222K	CERAMIC 2200PF K		
C66			CF92FV1H104J	MF 0.10UF J		
C67			CE04FW1H010M	ELECTRO 1.0UF 50WV		
C68			CE04FW1HR22M	ELECTRO 0.22UF 50WV		
C69			CK45FF1H223Z	CERAMIC 0.022UF Z		
C70			C91-0700-05	CERAMIC 0.1UF J		
C71			CK45FF1H223Z	CERAMIC 0.022UF Z		
C72			CF92FV1H682J	MF 6800PF J		
C76			CK45FF1H223Z	CERAMIC 0.022UF Z		
C77			C91-0700-05	CERAMIC 0.1UF J		
C78 ,79			CE04FW1C222M	ELECTRO 2200UF 16WV		
C80 ,81			CE04FW1A470M	ELECTRO 47UF 10WV		
C82 ,83			CE04FW0J471M	ELECTRO 470UF 6.3WV		
C84 ,85			CE04FW1E102M	ELECTRO 1000UF 25WV		
C86 ,87		⁎	CE04FW1C472M	ELECTRO 4700UF 16WV		
C88 ,89			CE04FW1V471M	ELECTRO 470UF 35WV		
C90			CK45FF1H223Z	CERAMIC 0.022UF Z		

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C91			CE04FW1C100M	ELECTRO 10UF 16WV		
C92			CE04FW1H0R1M	ELECTRO 0.1UF 50WV		
C100,101			CE04FW1C100M	ELECTRO 10UF 16WV		
C102			CC45FSL1H470J	CERAMIC 47PF J		
C103			CK45FB1H102K	CERAMIC 1000PF K		
C104			CC45FSL1H470J	CERAMIC 47PF J		
C105			CC45FSL1H180J	CERAMIC 18PF J		
C106			CE04W0J471M	ELECTRO 470UF 6.3WV		
C107			CE04W1A471M	ELECTRO 470UF 10WV		
C108			CF92FV1H224J	MF 0.22UF J		
C109,110		*	CQ93HP2A152J	MYLAR 1500PF J		
C111,112			CE04FW1A221M	ELECTRO 220UF 10WV		
C113,114			CQ09FS1H821JZS	POLYSTY 820PF J		
C115,116			CE04FW1C470M	ELECTRO 47UF 16WV		
C117,118			CQ09FS1H681JZS	POLYSTY 680PF J		
C119,120			C91-0161-05	POLYSTY 5PF F		
C121,122			CQ09FS1H391JZS	POLYSTY 390PF J		
C123,124			CQ09FS1H681JZS	POLYSTY 680PF J		
C127,128			CE04FW1C470M	ELECTRO 47UF 16WV		
C129			CE04FW0J471M	ELECTRO 470UF 6.3WV		
C130,131			CK45FF1H473Z	CERAMIC 0.047UF Z		
C132,133			CF92FV1H332J	MF 3300PF J	E	
C134			CK45FF1H103Z	CERAMIC 0.010UF Z	E	
⚠ C135,136			C91-0647-05	CERAMIC 0.01UF P		
C137,138			CF92FV1H152J	MF 1500PF J	E.	
C139,140			CE04HW1E100M	NP-ELEC 10UF 25WV		
C141			C91-0085-05	CERAMIC 0.022UF N		
240	2D		E11-0127-05	PHONE JACK (3P)		
244	2F		E13-0217-05	PHONO JACK (2P)		
245	2E		E23-0125-05	TERMINAL (GND)		
L1			L40-1092-14	SMALL FIXED INDUCTOR (1.0UH,M)		
L2			L79-0702-05	LINE FILTER		
L3 ,4		*	L79-0703-05	LC FILTER		
X1			L77-0587-05	CRYSTAL RESONATOR(37.500MHZ)		
B	2D,1F		N29-0035-05	PUSH RIVET (Ø3.5X5.5)		
C	1E		N29-0067-05	PUSH RIVET (Ø3.5X4.5)	E	
R32			RS14DB3D220J	FL-PROOF RS 22 J 2W		
R41			RS14DB3D220J	FL-PROOF RS 22 J 2W		
R63			RS14KB3D220J	FL-PROOF RS 22 J 2W		
R76		*	RS14DB3A1R5J	FL-PROOF RS 1.5 J 1W		
R125			RS14DB3D220J	FL-PROOF RS 22 J 2W		
R126			RS14DB3D330J	FL-PROOF RS 33 J 2W		
R163		*	RN14BK2C6811F	RN 6.81K F 1/6W		
R164		*	RN14BK2C6811F	RN 6.81K F 1/6W		
R167		*	RN14BK2C4641F	RN 4.64K F 1/6W		
R168		*	RN14BK2C4641F	RN 4.64K F 1/6W		
R169		*	RN14BK2C3161F	RN 3.16K F 1/6W		
R170		*	RN14BK2C3161F	RN 3.16K F 1/6W		
R171,172		*	RN14BK2C3831F	RN 3.83K F 1/6W		
R173,174		*	RN14BK2C6811F	RN 6.81K F 1/6W		
R175		*	RN14BK2C3161F	RN 3.16K F 1/6W		
R176		*	RN14BK2C3161F	RN 3.16K F 1/6W		
R177,178		*	RN14BK2C1212F	RN 12.1K F 1/6W		

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R179		*	RN14BK2C1782F	RN 17.8K F 1/6W		
R180		*	RN14BK2C1782F	RN 17.8K F 1/6W		
R181,182			RN14BK2C1003F	RN 100K F 1/6W		
R183,184		*	RN14BK2C2612F	RN 26.1K F 1/6W		
R185,186		*	RN14BK2C1001F	RN 1.00K F 1/6W		
R187,188		*	RN14BK2C1000F	RN 100.0 F 1/6W		
R189		*	RN14BK2C1003F	RN 100K F 1/6W		
R190			RN14BK2C1003F	RN 100K F 1/6W		
VR1			R12-3041-05	TRIMMING POT.(10K)OUTPUT		
VR2	2D	*	R10-4022-05	POTENTIOMETER(50K)PHONES LEVEL		
S1 -11	3D,3E		S40-1085-05	PUSH SWITCH (OPERATION SW)		
D1 ,2			GMA01	DIODE		
D1 ,2			1SS176	DIODE		
D3 ,4			RD4.7E(B2)	ZENER DIODE		
D5			GMA01	DIODE		
D5			1SS176	DIODE		
D6 ,7			RD4.7E(B2)	ZENER DIODE		
D8 -13			GMA01	DIODE		
D8 -13			1SS176	DIODE		
D14			1S2076	DIODE		
D15			RD4.7E(B2)	ZENER DIODE		
D16 -19			GMA01	DIODE		
D16 -19			1SS176	DIODE		
D20 -22			1S2076	DIODE		
D23			GMA01	DIODE		
D23			1SS176	DIODE		
D24 ,25			GMA01	DIODE		
D24 ,25			1SS176	DIODE		
D26 -29			1S2076	DIODE		
D30 -39			DSM1A1	DIODE		
D40 ,41			RD5.6E(B2)	ZENER DIODE		
D42			RD6.2E(B2)	ZENER DIODE		
D43			RD4.7E(B2)	ZENER DIODE		
D44			GMA01	DIODE		
D44			1SS176	DIODE		
D45			RD10E(B2)	ZENER DIODE		
D46			1S2076	DIODE		
D47			RD3.3E(B2)	ZENER DIODE		
D48			GMA01	DIODE		
D48			1SS176	DIODE		
D49			RD4.7E(B2)	ZENER DIODE		
D50 ,51			GMA01	DIODE		
D50 ,51			1SS176	DIODE		
D52			RD7.5J(B2)	ZENER DIODE		
D53			RD5.1J(B2)	ZENER DIODE		
D54 ,55			RD7.5J(B2)	ZENER DIODE		
D56			RD5.1J(B2)	ZENER DIODE		
D57			GMA01	DIODE		
D57			1SS176	DIODE		
D58 ,59			1S2076	DIODE		
D60 ,61			GMA01	DIODE		
D60 ,61			1SS176	DIODE		
D62			GMA01	DIODE		
D62			1SS176	DIODE		

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FL1	3D	*	CP2122GR	FLUORESCENT INDICATOR TUBE		
IC1			AN6555	IC(OP AMP X2)		
IC2 ,3			TA7256P	IC(OP AMP X2)		
IC4			AN6555	IC(OP AMP X2)		
IC5			AN6913	IC(COMPARATOR X2)		
IC5			TA75393S	IC(COMPARATOR X2)		
IC6			UPA80C	IC(7CH TRANSISTOR ARRAY)		
IC7		*	TRD5010	IC(KICK CONTROL)		
IC8			AN6913	IC(COMPARATOR X2)		
IC8			TA75393S	IC(COMPARATOR X2)		
IC9			TC40H000P	IC(NAND X4)		
IC10		*	UPD7519G-167-36	IC(MICROPROCESSOR)		
IC11			CX-20017	IC(16-BIT D/A CONVERTER)		
IC12			UPD4053BC	IC(3-INPUT 2CH MPX/DE-MPX)		
IC13		*	TL084CN	IC(OP AMP X4)		
IC14			NJM4560D-N	IC(OP AMP X2)		
IC15			UPC78L12	IC(VOLTAGE REGULATOR/ +12V)		
IC16		*	NJM79L12A	IC(VOLTAGE REGULATOR/ -12V)		
IC17			UPC4557C	IC(OP AMP X2)		
Q1 ,2			2SK301	FET		
Q3 -5			2SC2878	TRANSISTOR		
Q6 ,7			2SK301	FET		
Q8			2SC2878	TRANSISTOR		
Q9			2SK301	FET		
Q10 ,11			2SC2878	TRANSISTOR		
Q12			2SC1685(R,S)	TRANSISTOR		
Q12			2SC1815(Y,GR)	TRANSISTOR		
Q12			2SC945(A)(Q,P)	TRANSISTOR		
Q13			DTC144EFF	DIGITAL TRANSISTOR		
Q14			2SC1685(R,S)	TRANSISTOR		
Q14			2SC1815(Y,GR)	TRANSISTOR		
Q14			2SC945(A)(Q,P)	TRANSISTOR		
Q15			2SA1015(Y,GR)	TRANSISTOR		
Q15			2SA1127NC(R,S)	TRANSISTOR		
Q15			2SA733(A)(Q,P)	TRANSISTOR		
Q16			2SB514	TRANSISTOR		
Q17			2SD330	TRANSISTOR		
Q18			2SC1685(R,S)	TRANSISTOR		
Q18			2SC1815(Y,GR)	TRANSISTOR		
Q18			2SC945(A)(Q,P)	TRANSISTOR		
Q19 ,20			2SA1015(Y,GR)	TRANSISTOR		
Q19 ,20			2SA1127NC(R,S)	TRANSISTOR		
Q19 ,20			2SA733(A)(Q,P)	TRANSISTOR		
Q21		*	2SB605	TRANSISTOR		
Q22 -24			2SA1015(Y,GR)	TRANSISTOR		
Q22 -24			2SA1127NC(R,S)	TRANSISTOR		
Q22 -24			2SA733(A)(Q,P)	TRANSISTOR		
Q25			2SC1685(R,S)	TRANSISTOR		
Q25			2SC1815(Y,GR)	TRANSISTOR		
Q25			2SC945(A)(Q,P)	TRANSISTOR		
Q26 ,27			2SK105(F)	FET		
Q26 ,27			2SK246(Y)	FET		
Q28			2SK170(BL,V)	FET		
Q29			2SC1685(R,S)	TRANSISTOR		
Q29			2SC1815(Y,GR)	TRANSISTOR		

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Q29			2SC945(A)(Q,P)	TRANSISTOR		
Q30			2SA1015(Y,GR)	TRANSISTOR		
Q30			2SA1127NC(R,S)	TRANSISTOR		
Q30			2SA733(A)(Q,P)	TRANSISTOR		
Q31			2SK170(BL,V)	FET		
Q32 ,33			2SK152(3)	FET		
Q34 -37		⁎	2SK246(Y,GR)	FET		
Q38 -41			2SC2878	TRANSISTOR		
CONTROL CIRCUIT (MECHANISM) (X29-1610-00)						
C1			CF92FV1H473J	MF 0.047UF J		
C2			CK45FB1H222K	CERAMIC 2200PF K		
C3			CE04FW1H0R1M	ELECTRO 0.1UF 50WV		
C4			CF92FV1H333J	MF 0.033UF J		
C5			CK45FB1H102K	CERAMIC 1000PF K		
C6			CC45FSL1H470J	CERAMIC 47PF J		
C7			CC45FSL1H680J	CERAMIC 68PF J		
C8 ,9			CE04FW1C330M	ELECTRO 33UF 16WV		
C10			CK45FF1H103Z	CERAMIC 0.010UF Z		
C11 -13			CC45FSL1H220J	CERAMIC 22PF J		
C14 ,15			CE04FW1C330M	ELECTRO 33UF 16WV		
C16			CC45FSL1H680J	CERAMIC 68PF J		
C17			CF92FV1H333J	MF 0.033UF J		
C18			CF92FV1H682J	MF 6800PF J		
C19			CC45FSL1H101J	CERAMIC 100PF J		
C20			CF92FV1H333J	MF 0.033UF J		
C21			CK45FF1H103Z	CERAMIC 0.010UF Z		
C22 ,23			CE04FW1C101M	ELECTRO 100UF 16WV		
C24			CK45FF1H103Z	CERAMIC 0.010UF Z		
VR1			R12-1048-05	TRIMMING POT.(2K)TRACKING GAIN		
VR2 ,3			R12-4023-05	TRIM POT.(50K)FOCUS/TRACK ER		
VR4			R12-3057-05	TRIMMING POT.(10K)FOCUS GAIN		
D1			GMA01	DIODE		
D1			1SS176	DIODE		
D2 ,3			RD4.7E(B2)	DIODE		
D4 ,5			GMA01	DIODE		
D4 ,5			1SS176	DIODE		
IC1			TC40H004P	IC(INV BUFFER/CONVERTER X6)		
IC2			TC4011BP	IC(NAND X4)		
IC2			UPD4011BC	IC(NAND X4)		
IC3		⁎	CX-20109	IC(RF AMP FOR 3-BEAM PICK-UP)		
IC4			AN6555	IC(OP AMP X2)		
Q1			2SC1815(Y,GR)	TRANSISTOR		
Q1			2SC2320(E,F)	TRANSISTOR		
Q1			2SC945(A)(Q,P)	TRANSISTOR		
Q2			2SA1015(Y,GR)	TRANSISTOR		
Q2			2SA733(A)(Q,P)	TRANSISTOR		
Q2			2SA999(E,F)	TRANSISTOR		
Q3			2SC1815(Y,GR)	TRANSISTOR		
Q3			2SC2320(E,F)	TRANSISTOR		
Q3			2SC945(A)(Q,P)	TRANSISTOR		
Q4			2SD571	TRANSISTOR		
Q5			2SB514	TRANSISTOR		
Q6			2SK301	FET		

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				PROCESSOR CIRCUIT (X32-1020-00)		
C1			CK45FF1H223Z	CERAMIC 0.022UF Z		
C2			CK45FB1H821K	CERAMIC 820PF K		
C3			CK45FB1H681K	CERAMIC 680PF K		
C4			CF92FV1H473J	MF 0.047UF J		
C5			CF92FV1H102J	MF 1000PF J		
C6			CE04FW1C100M	ELECTRO 10UF 16WV		
C7		*	CC14SL1H390J	CERAMIC 39PF J		
C8			CK45FF1H223Z	CERAMIC 0.022UF Z		
C9			CC45FSL1H151J	CERAMIC 150PF J		
C10			CC45FSL1H680J	CERAMIC 68PF J		
C11			CK45FF1H223Z	CERAMIC 0.022UF Z		
C12			C91-0085-05	CERAMIC 0.022UF N		
C13			CK45FF1H223Z	CERAMIC 0.022UF Z		
C14 ,15			CC45FSL1H330J	CERAMIC 33PF J		
C16			C91-0085-05	CERAMIC 0.022UF N		
C17			CK45FF1H223Z	CERAMIC 0.022UF Z		
C18			CC45FSL1H151J	CERAMIC 150PF J		
J38	2F	*	E08-1503-05	RECTANGULAR RECEPTACLE (15P)		
L1			L32-0292-05	OSCILATING COIL		
L2			L40-1092-14	SMALL FIXED INDUCTOR (1.0UH,M)		
X1			L77-0586-05	CRYSTAL RESONATOR (8.4672MHZ)		
D1			RD8.2E(B2)	ZENER DIODE		
D2 -5			GMA01	DIODE		
D2 -5			1SS176	DIODE		
D6			1SV147	VARISTOR		
D7			GMA01	DIODE		
D7			1SS176	DIODE		
IC1			TD6315AP	IC(DATA SEPA CLK PULSE GEN PLL		
IC2			TC9178AF	IC(SYNC SEPA,EFM SIGNAL MPX)		
IC3			HM6116FP-4	IC(16K RAM)		
IC3			MB8418-20LPF	IC(16K RAM)		
IC4			TC9179F	IC(ERROR DETECTOR/CORRECTOR)		
Q1			2SA1015(Y,GR)	TRANSISTOR		
Q1			2SA1127NC(R,S)	TRANSISTOR		
Q1			2SA733(A)(Q,P)	TRANSISTOR		
Q2 ,3			2SC1685(R,S)	TRANSISTOR		
Q2 ,3			2SC1815(Y,GR)	TRANSISTOR		
Q2 ,3			2SC945(A)(Q,P)	TRANSISTOR		
Q4			2SC1923(Y)	TRANSISTOR		
				MEHCANISM ASS'Y (X92-1060-00)		
1	3B	*	A10-0757-12	CHASSIS CALKING ASSY		
2	1B	*	A11-0131-13	SUB CHASSIS CALKING ASSY		
3	2B	*	A11-0132-03	SUB CHASSIS		
4	2B	*	A11-0134-03	SUB CHASSIS		
8	2B	*	B09-0044-04	CAP		
C1			C91-0085-05	CERAMIC 0.022UF N		
12	1A	*	D10-1266-03	SLIDER (L)		
13	2B	*	D10-1267-03	SLIDER (R)		
14	1A	*	D10-1268-03	SLIDER (SUB CHASSIS CALK ASSY)		
15	2A		D10-1269-08	ARM		

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16	2B	⁎	D10-1270-04	ROD		
17	1B	⁎	D10-1271-03	ARM		
18	1A	⁎	D12-0105-15	CAM		
19	3B		D13-0159-08	GEAR		
20	3A		D13-0160-08	GEAR		
21	2A	⁎	D13-0161-03	GEAR		
22	2A		D13-0162-08	GEAR		
23	2A		D13-0163-08	GEAR		
24	2B	⁎	D13-0164-04	GEAR		
25	3A,3B	⁎	D14-0106-04	ROLLER		
26	3A	⁎	D14-0107-04	ROLLER		
27	3B		D15-0220-08	PULLEY		
28	3B		D16-0104-08	BELT		
29	1B	⁎	D21-1051-04	SHAFT		
30	1B	⁎	D21-1052-04	SHAFT		
31	1A	⁎	D32-0122-04	STOPPER		
32	3B	⁎	D40-0314-05	DRIVE MECHANISM ASSY		
33	2A	⁎	D40-0315-05	DRIVE MECHANISM ASSY		
37	3A	⁎	F19-0348-04	BLIND PLATE		
41	1B,3B		G01-0675-04	TORSION COIL SPRING		
42	1A,1B	⁎	G01-1523-04	EXTENSION SPRING		
43	2B	⁎	G01-1524-04	EXTENSION SPRING		
44	2A	⁎	G01-1525-04	EXTENSION SPRING		
45	2A,2B	⁎	G13-0166-04	CUSHION		
49	2A,2B	⁎	J02-0158-05	INSULATOR		
50	2B	⁎	J02-0163-05	INSULATOR		
51	1A	⁎	J11-0066-04	CLAMPER		
52	2B	⁎	J19-2153-04	HOLDER (ROD)		
53	3A		J21-3507-08	MOUNTING HARDWARE ASSY		
54	2A	⁎	J21-3509-03	MOUNTING HARDWARE ASSY		
55	2A		J21-3511-08	MOUNTING HARDWARE ASSY		
56	2B	⁎	J21-3513-04	MOUNTING HARDWARE		
57	2B	⁎	J21-3514-03	MOUNTING HARDWARE		
58	2A	⁎	J25-4460-03	PRINTED WIRING BOARD		
59	3B	⁎	J31-0233-05	COLLAR (⌀4X10)		
60	3A	⁎	J90-0143-03	GUIDE		
61	1A	⁎	J90-0144-03	RAIL		
63	1B	⁎	J99-0024-02	TRAY		
64	2B	⁎	J99-0025-03	TRAY		
65	2B	⁎	J99-0026-03	TRAY		
-			J61-0070-05	WIRE BAND		
-			J61-0307-05	WIRE BAND		
J	2A,2B		N09-0976-05	TAPTITE SCREW (M3X6)		
K	2A,2B	⁎	N09-1379-05	STEPPED SCREW (M2.6X15)		
L	2A,2B	⁎	N09-1380-05	STEPPED SCREW (M2.6X5)		
M	3B	⁎	N09-1381-05	STEPPED SCREW (M5X26)		
N	3A,2B	⁎	N09-1431-05	TAPTITE SCREW (M2X6)		
P	3A		N29-0067-05	PUSH RIVET (⌀3.5X4.5)		
Q	1A,1B		N29-0207-04	RETAINING RING (⌀2.5)		
R	3B		N29-0220-05	RETAINING RING (⌀2.4)CS		
S1 ,2	3A,2B	⁎	S46-1045-05	LEAF SWITCH		
S3	2A	⁎	S46-1046-05	LEAF SWITCH		

E: Scandinavia & Europe H:Audio Club K: USA P: Canada

S: South Africa T: England U: PX(Far East, Hawaii)

UE: AAFES(Europe) X: Australia M: Other Areas

⚠ indicates safety critical components.

※ New Parts

10. PARTS LIST

Parts without **Parts No.** are not supplied.
Les articles non mentionnes dans le **Parts No.** ne sont pas fournis.
Teile ohne **Parts No.** werden nicht geliefert.

Ref. No. 参照番号	Address 位置	New Parts 新	Parts No. 部品番号	Description 部品名／規格	Desti- nation 仕向	Re- marks 備考
84	3A		T42-0049-15	MOTOR ASSY		
85	2A		T42-0051-08	MOTOR ASSY		
86	2A	*	T42-0053-04	MOTOR ASSY		
87	1A	*	T50-1023-04	YOKE		
88	1A	*	T99-0222-05	MAGNET		

E Scandinavia & Europe H:Audio Club K: USA P: Canada
S: South Africa T: England U: PX(Far East, Hawaii)
UE AAFES(Europe) X: Australia M: Other Areas

⚠ indicates safety critical components.

11. SPECIFICATIONS

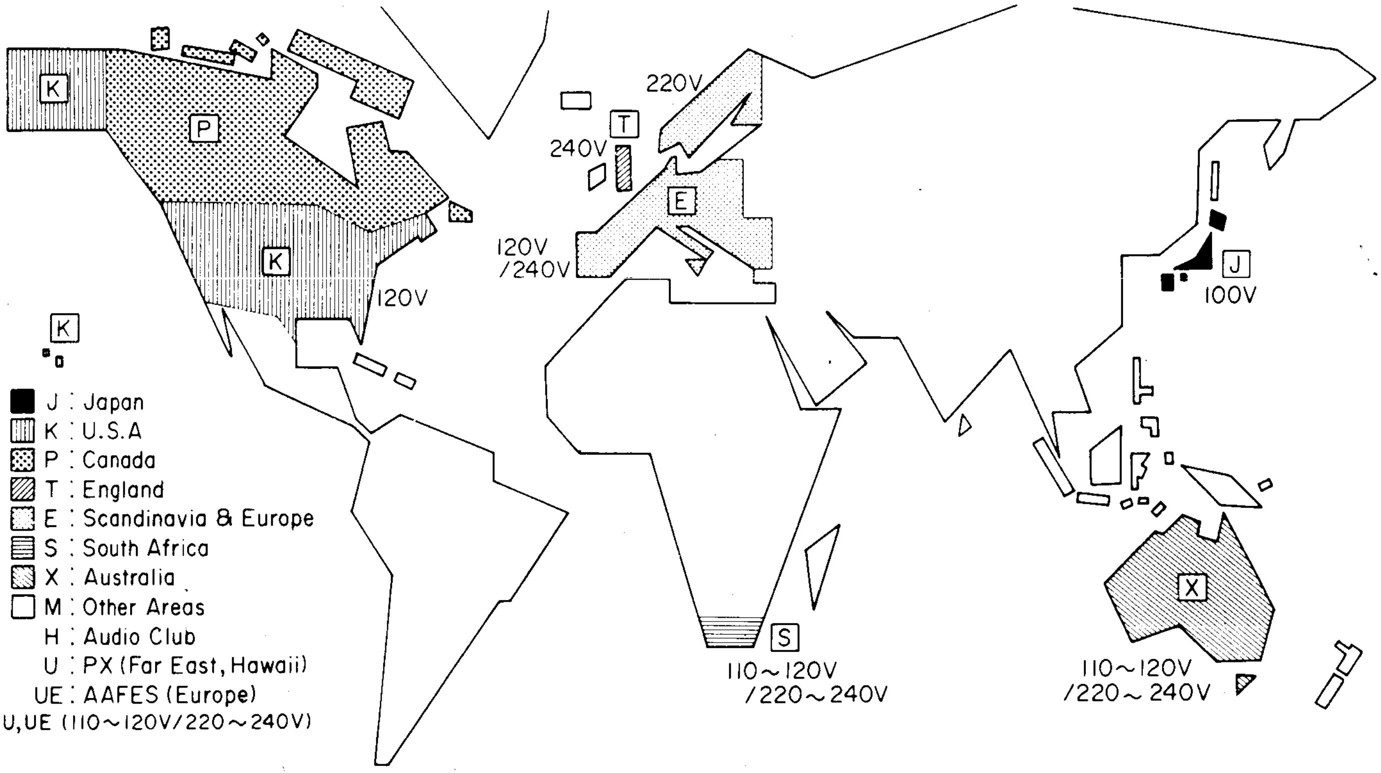
Number of channels	2 channels
Frequency response	4 Hz — 20 kHz, +0.5 dB −1.0 dB
Dynamic range	95 dB
Total harmonic distortion	0.002% at 1 kHz
Channel separation	90 dB at 1 kHz
Wow & flutter	Unmeasurable limit
Line output level	2.0 V
Headphones output level/impedance	31 mW/32 ohms
Spindle speed	500 ~ 200 rpm (CLV)
Quantization	16 bits linear 1 channel
Sampling Frequency	44.1 kHz
Channel modulation code	EFM (eight to fourteen modulation)
Pick up type	Optical pick up
Laser type	Semiconductor laser
Power requirements	120 V, 60Hz...USA & Canada models, 120 V/220 — 240 V, 50/60 Hz (Switchable)...other countries
Power consumptions	16 W
Dimentions	W 440 mm (17-5/16″) H 88 mm (3-15/32″) D 310 mm (12-7/32″)
Weight	6.0 kg (13.2 lb)
Supplied accessories	Connection cables

Kenwood follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Kenwood poursuit une politique de progrès constants en ce qui doncerne le développement. Pour cette raison, les spécifications sont sujettes à modifications sans préavis.

Kenwood strebt ständige, Verbesserungen in der Entwicklung an. Daher bleiben Änderungen der technischen Daten jederzeit vorbehalten.

12. WORLD MAP & AREA CODE


K
P
K
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K
220V
T
240V
E
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J
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S
110~120V
/220~240V
X
110~120V
/220~240V
■ J : Japan
▥ K : U.S.A
▩ P : Canada
▨ T : England
▒ E : Scandinavia & Europe
▤ S : South Africa
▧ X : Australia
☐ M : Other Areas
H : Audio Club
U : PX (Far East, Hawaii)
UE : AAFES (Europe)
U, UE (110~120V/220~240V)

Note:

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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